Cyborg 16H Schematic

Intel TGL-H DVT

2020/10/06

https://vinafix.com

REV : X01

DY : None Installed
DIS: DISCRTE OPTIMUS installed

TGL-H

Wistron Corporation
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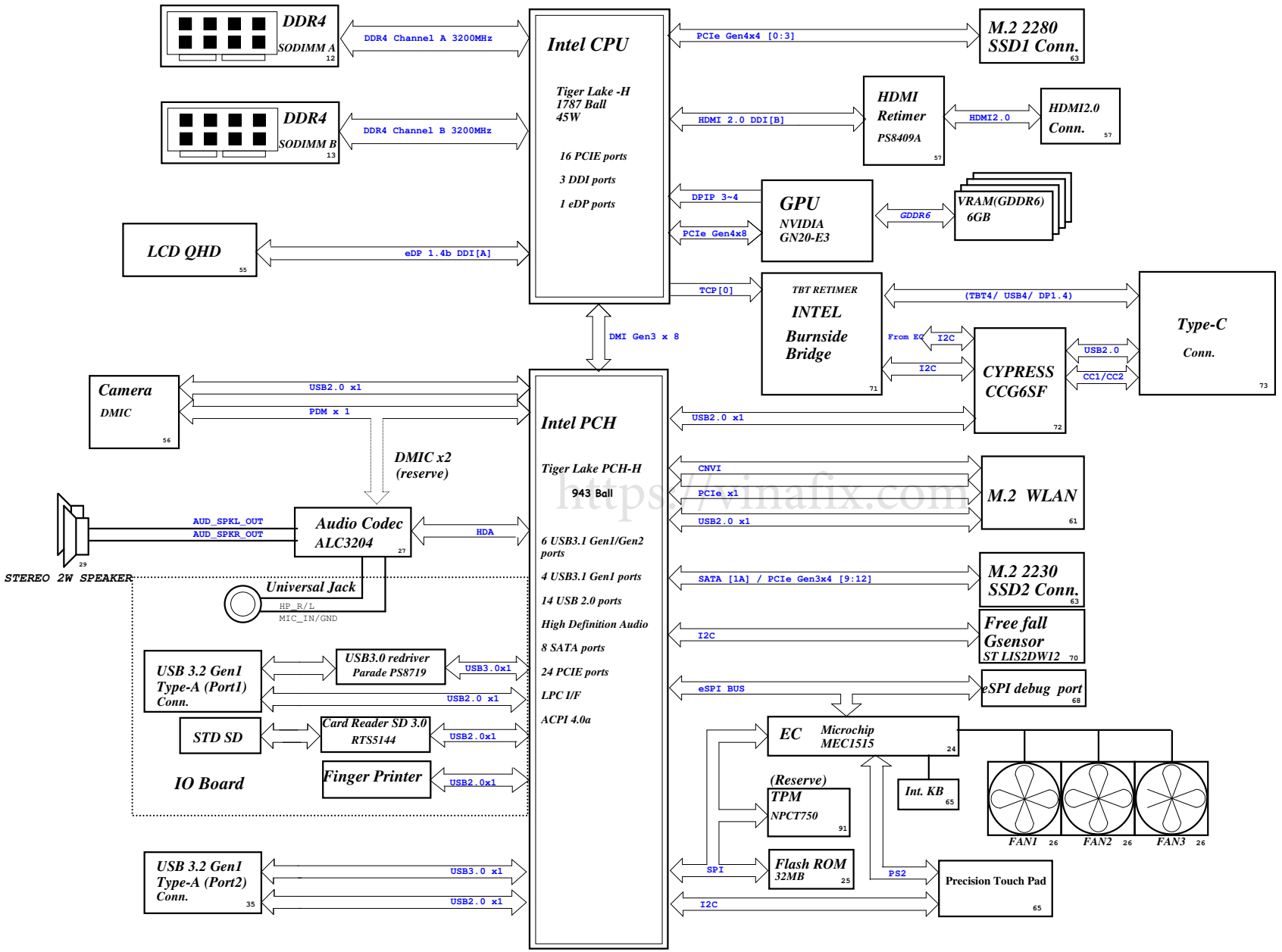
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*		
Size: A4	Document Number: Cyborg_TGL-H RTX	Rev: X01
Date: Friday, November 20, 2020	Sheet 1 of 106	

Project Code : QRQY00000944
PCB P/N : 19843-SA
Revision : X00

Cyborg TGL-H RTX Block Diagram



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CHARGER ISL9538 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC SY8288CRAC-GP 45 TPS51393PRJER-GP	
INPUTS	OUTPUTS
DCBATOUT	3D3V_PWR 3D3V_S5 5V_PWR 5V_S5

CPU Core Power NCP81307MNTXG-GP 46~50 NCP302045MNTWG*4 RT6543AGQW-GP	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT	+VCCSA

DDR4 SUS TPS51486RJER-GP 51	
INPUTS	OUTPUTS
DCBATOUT 3D3V_S5	1D2V_S3 0D6V_S0 2D5V_S3

CPU VCCPRIM_CORE 1V 11	
INPUTS	OUTPUTS
1D0V_S5	+VCCPRIM_CORE

CPU DCDC-V1D00A AOZ2262QI-10-GP-U 53	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D8V APL5934KAI-TRG-GP-U 54	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0 G2898KD1U-GP 40	
INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

1D8V_AON_S0 G2898KD1U-GP 86	
INPUTS	OUTPUTS
3D3V_S0	1D8V_AON_S0

1V_VGACORE_S0 MP2884AGU-0916-GP 85	
INPUTS	OUTPUTS
DCBATOUT	1V_VGACORE_S0

1V_VGA_S0 TPS51396RJER-GP 86	
INPUTS	OUTPUTS
DCBATOUT	1V_VGA_S0

1D35V_VGA_S0 RT8816BGQW-GP 86	
INPUTS	OUTPUTS
DCBATOUT	1D35V_VGA_S0

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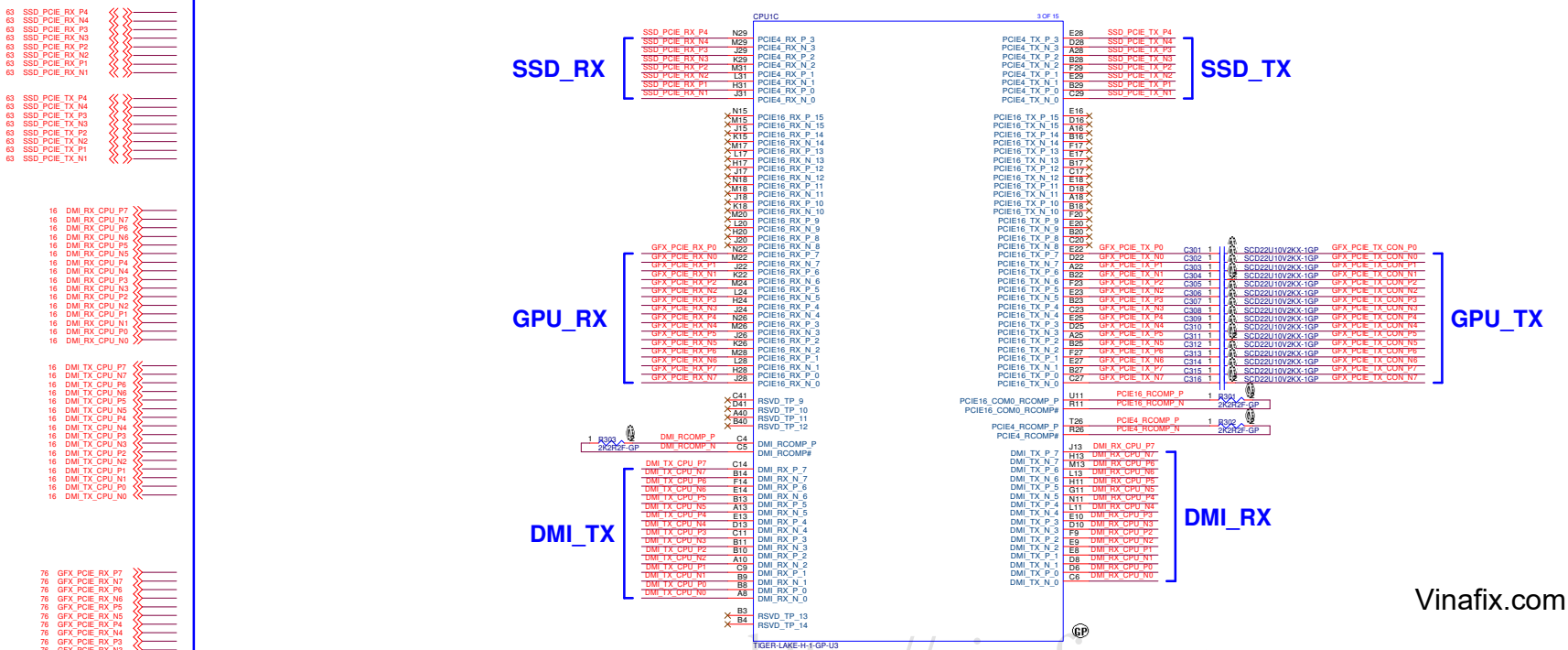
Title: Block Diagram

Size: Custom	Document Number: Cyborg_TGL-H RTX	Rev: X01
Date: Friday, November 20, 2020	Sheet 2 of 106	



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575683_TGL_EDS_Vol1_Rev1p0 P.108

Table 7-2. PCI Express* 16-lane Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width 0:1:0	0:1:1	0:1:2	CFG Signals CFG [6]	CFG [5]	CFG [2]	Lanes 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
PCIe Controller							GPU PCIe 011								PCIe 010							
2x8 **Reversed**	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
PCIe Controller							PCIe 010								PCIe 011				PCIe 012			
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
PCIe Controller							PCIe 012				PCIe 011				PCIe 010							
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

618429_TGL_H_PDG_Rev1p0 RCOMP

Pin Name	PCIE4_RCOMP_P PCIE4_RCOMP_N	PCIE16_COM0_RCOMP_P PCIE16_COM0_RCOMP_N	DMI_RCOMP_P DMI_RCOMP_N
Board Rterm (ohm)	2.2KΩ±1% Differential	2.2KΩ±1% Differential	2.2KΩ±1% Differential
Board Rdc (ohm)	<0.5 sum both traces	<0.5 sum both traces	<0.5 sum both traces
Board Cap (pF)	2	2	N/A
Spacing for Breakout (um)	MS: 500 SL/DSL: 380	MS: 500 SL/DSL: 380	MS: 500 SL/DSL: 380
Spacing for Mainroute (um)			
DDR			
HDMI			
DP			
eDP			
DSI			
CSI			
Type-C			
PCIe4 x4	X		
PCIe4 x16		X	
DMI			X
DPIP[0/1/2/3]			
ModPHY			
USB2			
GPIO_1.8V/3.3V			
SoundWire			
GPIO_1.8V			
XTAL			
CNVI_DPHY			

Dell_CY21_CSB_HSIO_Port_Assignment_Rev0.1_2020-04-07_Cyborg-H

Ball	HSIO Lane	HSIO Type and Lane	DDI TCP0	USB3 support up to SuperSpeed	DP up to HBR3, HDMI up to 5.94	CY21 Port Mapping	Cyborg-H
BN38	0	USB-C 0				TBT #0	TBT #0
J31	4	PCIe 4.0 #0					
L31	5	PCIe 4.0 #1				PCIe x 4 <Gen4> (NVMe storage)	CPU M.2 SSD <Gen4> (PCIex4)
K29	6	PCIe 4.0 #3					PCIe x 4 <Gen4> (NVMe storage)
M29	7	PCIe 4.0 #4					
J28	4	PCIe 16 #0					
L28	5	PCIe 16 #1					
K26	6	PCIe 16 #2					
M26	7	PCIe 16 #3				dGPU (x8)	dGPU (x8)
J24	4	PCIe 16 #4					
L24	5	PCIe 16 #5					
K22	6	PCIe 16 #6					
M22	7	PCIe 16 #7					
						PCIe x 16	

Ball	PCH HSIO Lane	HSIO Type and Lane	CY21 Port Mapping	Cyborg-H
L24	14	DMI 7	DMI	DMI x 8
P22	15	DMI 6		
R26	16	DMI 5		
H26	17	DMI 4		
J26	18	DMI 3		
L29	19	DMI 2		
H30	20	DMI 1		
L31	21	DMI 0		

TGL-H

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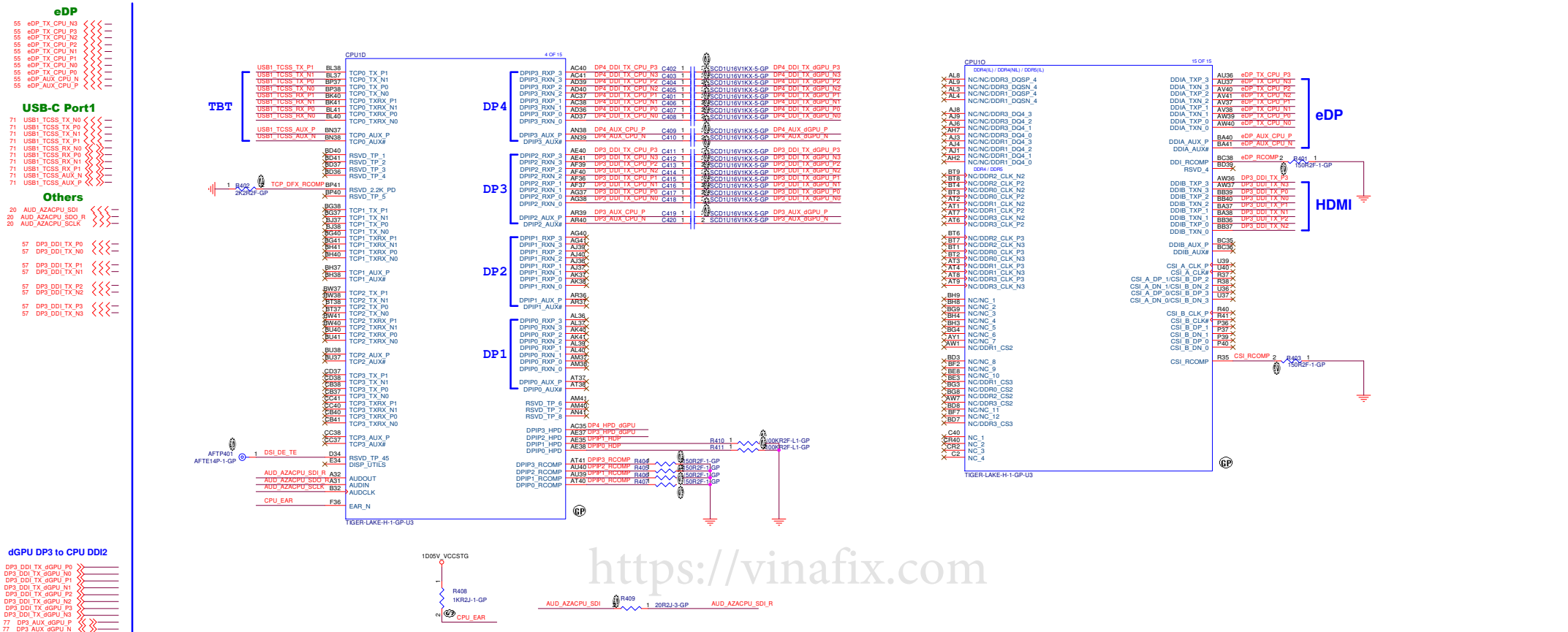
Title: CPU (PEG/DMI/PCIE4.0)

Size: A2 | Document Number: Cyborg_TGL-H RTX | Rev: X01

Date: Friday, November 20, 2020 | Sheet 3 of 106

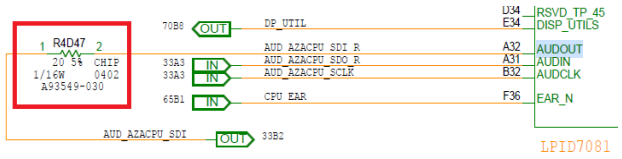


618429_TGL_H_PDG_Rev1p0 P.136

Table 64. CFG Signals Functionality and Termination

CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted:	Pull-up to VCCSTG	1K ohm
			continued...
CFG	**Description**	**Termination**	**Resistor**
	- 1 = (Default) Normal Operation; No stall. - 0 = Stall		

618697_TGL_H_DDR4_SCH_REV1P1 P.13



618429_TGL_H_PDG_Rev1p0 RCOMP

Pin Name	DDI_RCOMP	CSI_RCOMP	TC_RCOMP_P TC_RCOMP_N	TCP0_MBIAS_RCOMP_P	DPIP[0/1/2/3]_RCOMP
Board Rterm (ohm)	150Ω±1% to GND	150Ω±1% to GND	150Ω±1% Differential	2.2kΩ±1% to GND	150Ω±1% to GND
Board Rdc (ohm)	<0.2	<0.5	<0.5 swn both traces	<0.5	<0.5
Board Cap (pF)	N/A	N/A	N/A	2	N/A
Spacing for Breakout (um)	MS: 500	MS: 500	MS: 500	MS: 500	MS: 500
Spacing for Mainroute (um)	SL/DSL: 380	SL/DSL: 380	SL/DSL: 380	SL/DSL: 380	SL/DSL: 380
DDR					
HDMI	X				
DP	X				
eDP	X				
DSI	X				
CSI		X			
Type-C			X	X	
PCIe4 x4					
PCIe4 x16					
DMI					
DPIP[0/1/2/3]					X
ModPHY					
USB2					
GPIO_1.8V/3.3V					
SoundWire					
GPIO_1.8V					
XTAL					
CNVi_DPHY					

575683_TGL_EDS_Vol1_Rev1p0 P.115

Table 9-1. Display Ports Availability and Link Rate for UP4/UP3/H-Processor Lines

Port	UP4-Processor Line	UP3-Processor Line	H-Processor Line
DDI A[1,2]	eDP* up to HBR3 MIPI DSI up to 2.5 Gbps	eDP* up to HBR3 MIPI DSI up to 2.5 Gbps[5]	eDP* up to HBR3
DDI B[2]	eDP* up to HBR3 DP* up to HBR2 HDMI* up to 5.94 Gbps MIPI DSI up to 2.5 Gbps	eDP* up to HBR3 DP* up to HBR2 HDMI* up to 5.94 Gbps	eDP* up to HBR3 DP* up to HBR2 HDMI* up to 5.94 Gbps
DDI TCP0[3]	DP* up to HBR3 HDMI* up to 5.94 Gbps	DP* up to HBR3 HDMI* up to 5.94 Gbps	DP* up to HBR3 HDMI* up to 5.94 Gbps
DDI TCP1[3]	DP* up to HBR3 HDMI* up to 5.94 Gbps	DP* up to HBR3 HDMI* up to 5.94 Gbps	DP* up to HBR3 HDMI* up to 5.94 Gbps
DDI TCP2[3]	DP* up to HBR3 HDMI* up to 5.94 Gbps	DP* up to HBR3 HDMI* up to 5.94 Gbps	DP* up to HBR3 HDMI* up to 5.94 Gbps
DDI TCP3[3]	N/A	DP* up to HBR3 HDMI* up to 5.94 Gbps	DP* up to HBR3 HDMI* up to 5.94 Gbps
DPIP0[4]	N/A	N/A	DP* up to HBR3
DPIP1[4]			DP* up to HBR3
DPIP2[4]			DP* up to HBR3
DPIP3[4]			DP* up to HBR3

Dell_CY21_CSB_HSIO_Port_Assignment_Rev0.1_2020-04-07_Cyborg-H

Ba	HSIO La	HSIO Type and Lane				CY21 Port Mapping	Cyborg-H
BN38	0	USB-C 0	DDI TCP0	USB3 support up to SuperSpeed	DP up to HBR3, HDMI up to 5.94	TBT #0	TBT #0
BA41	Display Interfaces	DDI A		eDP up to HBR3 DP up to HBR3	MIPI_1 up to 2.5 Gbps HDMI up to *2.1	eDP	eDP
BC36		DDI B					HDMI2.0
AT38		DPIP0		DP up to HBR3		DPIN0	
AR37		DPIP1				DPIN1	
AR40		DPIP2				DPIN2	
AN39		DPIP3				DPIN3	

TGL-H

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Title: CPU (DDI/EDP/TCP/DP/CSI)

Size: A2 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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618429_TGL_H_PDG_Rev1p0 RCOMP

Pin Name	DDR_RCOMP
Board Rterm (ohm)	100Ω ±1% to GND
Board Rdc (ohm)	<0.05
Board Cap (pF)	N/A
Spacing for Breakout (um)	TGL-U: 500
Spacing for Manuroute (um)	
DDR	X
HDMI	
DP	
eDP	
DSI	
CSI	
Type-C	
PCIe4 x4	
PCIe4 x16	
DMI	
DPIP[0/1/2/3]	
MoPHY	
USB2	
GPIO_1.8V/3.3V	
SoundWire	
GPIO_1.8V	
XTAL	
CNVi_DPHY	

575683_TGL_EDS_Vol1_Rev1p0 P.98

Figure 5-2. DDR4 Interleave (IL) and Non-Interleave (NIL) Modes Mapping

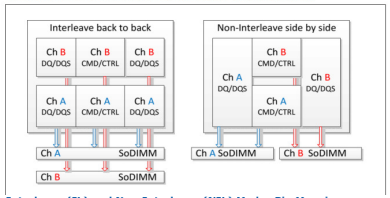
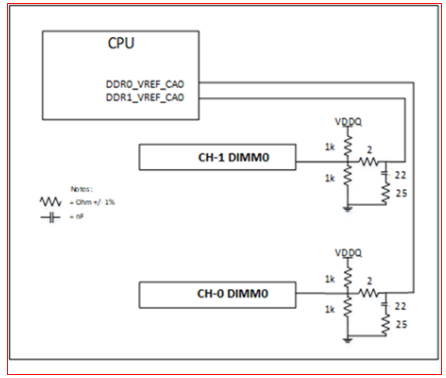


Table 5-16. Interleave (IL) and Non-Interleave (NIL) Modes Pin Mapping

IL (DDR4)		NIL (DDR4)		NIL (LPDDR4x)	
Channel	Byte	Channel	Byte	Sub Channel	Byte
DDR0	Byte0	DDR0	Byte0	DDR7	Byte1
DDR0	Byte1	DDR0	Byte2	DDR6	Byte0
DDR0	Byte2	DDR0	Byte4	DDR7	Byte1
DDR0	Byte3	DDR0	Byte6	DDR6	Byte0
DDR0	Byte4	DDR1	Byte0	DDR5	Byte1
DDR0	Byte5	DDR1	Byte2	DDR4	Byte0
DDR0	Byte6	DDR1	Byte4	DDR5	Byte1
DDR0	Byte7	DDR1	Byte6	DDR4	Byte0
DDR1	Byte0	DDR0	Byte1	DDR3	Byte1
DDR1	Byte1	DDR0	Byte3	DDR2	Byte0
DDR1	Byte2	DDR0	Byte5	DDR3	Byte1
DDR1	Byte3	DDR0	Byte7	DDR2	Byte0
DDR1	Byte4	DDR1	Byte1	DDR1	Byte1
DDR1	Byte5	DDR1	Byte3	DDR0	Byte0
DDR1	Byte6	DDR1	Byte5	DDR1	Byte1
DDR1	Byte7	DDR1	Byte7	DDR0	Byte0

618429_TGL_H_PDG_Rev1p0 DDR4 1DPC SODIMM



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Title: CPU (DDR)

Size	Document Number	Rev
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19 BCLK_CLK_PCH_P
19 BCLK_CLK_PCH_N
19 PCIBCLK_CLK_PCH_P
19 PCIBCLK_CLK_PCH_N
46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERT#_CPU
20,24,44,46,72 PROCHOT#_CPU
19 CPU_RTC_CLK
18 THERMTRIP_CPU_N
17 CPU_SYNC
17 CPU_DOWN
17 CPU_PLT_RST_N
17,24 PECI_PCH
19 CPU_PWRGD

JTAG

19 CPU_JTAG_TRST_N
20 CPU_JTAG_TMS
20 CPU_JTAG_TDO
20 CPU_JTAG_TDI
20 CPU_JTAG_TCK
17 CPU_JTAG_PREQ_N
17 CPU_JTAG_PRDY_N

19 PCH_CPU_NSSC_CLK_DP
19 PCH_CPU_NSSC_CLK_DN
22,40 VCCST_OVERRIDE
40 ALL_SYS_PWRGD
19 CPU_WAKE
18 PCH_2_CPU_TRIGGER
18 CPU_2_PCH_TRIGGER

XDP

1D05V_VCCSTG
R609 1KR2F-L1-GP PROCHOT#_CPU
3D3V_S5
R604 10KR2F-2-GP CPU_ID
1D05V_VCCST
R607 56R2J-4-GP SVID_ALERT#_CPU
R601 100R2F-L1-GP-U SVID_DATA_CPU
R617 1KR2F-3-GP CPU_CATERR_N
1D05V_VCCIO_OUT
R613 SRN10KJ-5-GP BPM_N3 BPM_N2
R612 SRN10KJ-5-GP BPM_N1 BPM_N0
20191024_Ricky
R605 100R2F-GP-U CPU_JTAG_PRDY_N
XDP
20191023_Ricky
1D05V_VCCSTG
R632 51R2J-2-GP CPU_JTAG_PREQ_N
R635 51R2J-2-GP CPU_JTAG_TDI
R636 51R2J-2-GP CPU_JTAG_TMS
20190425_Byron
R633 51R2J-2-GP CPU_JTAG_TDO
R634 51R2J-2-GP CPU_JTAG_TCK

618697_TGL_H_DDR4_SCH_REV1P1 P.29.30

16CS BI H_PROCHOT_CPU_N R4C45 499 1% 0603 CHIP A93550-053
16CS IN CO_ST_VIDALERT_N R4E6 0 5% 0402 CHIP A93549-001
16CS OUT H_PMEN R2E12 20 5% 1/16W 0402 A93549-030
R2E11 5K EMPTY 0402 A93549-016
CAD NOTE: PLACE NEAR CPU

618429_TGL_H_SchChk_Rev1p0 P.20

Pin Name	System Pull-up/ Pull-down
PECI	33Ω series resistor to EC, 13 Ohm resistor to PCH

618429_TGL_H_PDG_Rev1p0 RCOMP

Pin Name	TC_RCOMP_P TC_RCOMP_N
Board Rterm (ohm)	150Ω±1% Differential
Board Rdc (ohm)	<0.5 sum both traces
Board Cap (pF)	N/A
Spacing for Breakout (um)	MS: 500
Spacing for Mainroute (um)	SL/DSL: 380
DDR	
HDMI	
DP	
eDP	
DSI	
CSI	
Type-C	X
PCIe4 x4	
PCIe4 x16	
DMI	
DPIF[0/1/2/3]	
ModPHY	
USB2	
GPIO_1 @V3.3V	
SoundWire	
GPIO_1 @V	
XTAL	
CNVI_DPHY	

Follow XPS & NTD 7/27
3D3V_S5 C601 SCD1U16V2KX-3DLGP
1D05V_VCCST R623 1KR2F-3-GP
U601 74LVC1G07GW-GP
NC#1 VCC A GND Y
ALL_SYS_PWRGD VCCST_PWRGD R622 62R2F-GP VCCST_PWRGD_R
73.01G07.0HG

CPU1E 5 OF 15
BCLK_CLK_PCH_P C36 BCLK_P
BCLK_CLK_PCH_N D36 BCLK#
PCIBCLK_CLK_PCH_P C37 PCI_BCLK_P
PCIBCLK_CLK_PCH_N B37 PCI_BCLK_N
SVID_DATA_CPU D32 VIDSOUT
SVID_CLK_CPU E32 VIDSCK
SVID_ALERT#_CPU R618 0R2J-2-GP E32 VIDALERT#
PROCHOT#_CPU R608 499R2F-2-GP H35 PROCHOT#
CPU_RTC_CLK CR22 RTC_CLK
THERMTRIP_CPU_N F34 THERMTRIP#
CPU_SYNC CR23 PM_SYNC
CPU_DOWN R602 20R2F-GP CPU_DOWN_R CR24 PM_DOWN
CPU_PLT_RST_N CR25 DRAM_RESET#
PECI_PCH CR26 PECI
CPU_PWRGD PROCPWRGD
CPU_CATERR_N H36 CATERR#
BPM_N3 H39 BPM#_3
BPM_N2 H40 BPM#_2
BPM_N1 G38 BPM#_1
BPM_N0 H37 BPM#_0
CPU_JTAG_TRST_N E40 PROC_TRST#
CPU_JTAG_TMS G41 PROC_TMS
CPU_JTAG_TDO G39 PROC_TDO
CPU_JTAG_TDI F39 PROC_TDI
CPU_JTAG_TCK G40 PROC_TCK
F37 RSVD_1
E37 RSVD_2
R610 150R2F-1-GP TC_RCOMP_P BR41 TC_RCOMP_P
TC_RCOMP_N BR40 TC_RCOMP#
PCH_CPU_NSSC_CLK_DP C39 CLK_XTAL_P
PCH_CPU_NSSC_CLK_DN D39 CLK_XTAL#
TIGER-LAKE-H-1-GP-U3

RSVD_18 CT3 CPU_ID
CFG_15 J40
CFG_14 L41 CPU_CFG14
CFG_13 J41
CFG_12 N41
CFG_11 L40 CPU_CFG11
CFG_10 N40 CPU_CFG10
CFG_9 M39 CPU_CFG9
CFG_8 J37
CFG_7 M38 CPU_CFG7
CFG_6 J38 CPU_CFG6
CFG_5 J35 CPU_CFG5
CFG_4 N39 CPU_CFG4
CFG_3 L37 CPU_CFG3
CFG_2 M35 CPU_CFG2
CFG_1 M37
CFG_0 N36
XDP
CFG_17 M41 CPU_STB_P1 1 AFTP601 AFTE14P-1-GP NTD Connect to XDP XPS NC
CFG_16 L39 CPU_STB_P0 1 AFTP602 AFTE14P-1-GP
PROC_PREQ# H34 CPU_JTAG_PREQ_N
PROC_PRDY# G36 CPU_JTAG_PRDY_N
CFG_RCOMP A34 CFG_RCOMP R605 49D9R2F-GP
VCCSTPWRGOOD_TCSS CP23 VCCSTPWRGOOD_TCSS R611 0R2J-2-GP VCCST_OVERRIDE
VCCST_PWRGD CP24 VCCST_PWRGD_R
SKTOCC# CR3 SKTOCC_N 1 TP601
CPU_WAKE CU23 CPU_WAKE

TP602 1 TP_CPU_EXTBGREF H41
PCH_2_CPU_TRIGGER CT23
CPU_2_PCH_TRIGGER R618 0R2J-2-GP CPU_2_PCH_TRIGGER_R CT24
CN24 CM25 CR31 CN25 CM24 CR29

CPU1M 13 OF 15
RSVD_TP_46 BG33
RSVD_TP_15 BG12
RSVD_TP_25 BE33
RSVD_TP_26 BE12
RSVD_TP_27 BD33
RSVD_TP_16 BD12
RSVD_TP_17 BA33
RSVD_TP_28 BA12
RSVD_TP_29 AY33
RSVD_TP_18 AY12
RSVD_TP_30 AV33
RSVD_TP_31 AV12
RSVD_TP_32 BT33
IST_TP_1 AG11
IST_TP_0 AM33
RSVD_TP_33 BP11
RSVD_TP_34 BR33
RSVD_TP_44 BR12
RSVD_TP_35 BN33
RSVD_TP_43 BN12
RSVD_TP_36 BR11
RSVD_TP_37 BR12
PROC_TRIGIN BN11
PROC_TRIGOUT RSVD_TP_38 BN12
RSVD_TP_39 BN13
RSVD_TP_19 AG13
RSVD_TP_40 AG12
RSVD_TP_20 RSVD_TP_41 AF13
RSVD_TP_21 RSVD_TP_42 AF12
RSVD_TP_22 BM33
RSVD_TP_23 RSVD_7 P31
RSVD_TP_24 RSVD_8 T29
RSVD_9 CP22
RSVD_10 CU22
RSVD_11 CU21
RSVD_12 CU22
RSVD_13 R28
RSVD_14
TIGER-LAKE-H-1-GP-U3

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS

CFG2
1: (DEFAULT)NORMAL OPERATION;
0: LANE REVERSAL

CPU_CFG2 R626 1KR2J-1-GP

DFX ENABLED BIT IN DEBUG INTERFACE MSR

CFG3
1 : DISABLED
0 : ENABLED

CPU_CFG3 R629 1KR2J-1-GP

eDP enable Strap

CFG4
1:Disable
0:Enable

CPU_CFG4 R627 1KR2J-1-GP

PCIE PORT BIFURCATION STRAPS

CFG[6:5]
11: x16 - DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED
10: x8, x8 - DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED
01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED
00: x8, x4, x4 - DEVICE 1 FUNCTION 1 ENABLED,
DEVICE 1 FUNCTION 2 ENABLED

CPU_CFG5 R624 1KR2J-1-GP
CPU_CFG6 R625 1KR2J-1-GP

PEG DEFER TRAINING

CFG7
1: (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XXRESETB DE ASSERTION
0 = PEG Wait for BIOS for training.

CPU_CFG7 R628 1KR2J-1-GP

CFG[9:11]

CFG	Description	Termination	Resistor
CFG[11:9]		Pull-up to VCCIO	1K ohm

1D05V_VCCIO_OUT
R630 1KR2J-1-GP CPU_CFG9
R637 1KR2J-1-GP CPU_CFG10
R638 1KR2J-1-GP CPU_CFG11

PEG60 Lane Reversal

CFG14
1: default disable
0: enable

CPU_CFG14 R631 1KR2J-1-GP

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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SVID/CLK/XDP/FIVR/THERM)
Size: A2 | Document Number: Cyborg_TGL-H RTX | Rev: X01
Date: Friday, November 20, 2020 | Sheet 6 of 106

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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCCIN)

Size: A3 | Document Number: Cyborg_TGL-H RTX | Rev: X01

Date: Friday, November 20, 2020 | Sheet 7 of 106

34~48A

1D8V_VCCIN_AUX

CPU1L 12 OF 15

TIGER-LAKE-H-1-GP-U3

For BPM, XDP

970mA

1A

340mA

0.5A

4.3A

CPU1N 14 OF 15

1D2V_S3

2A

1D8V_PCH_C10

0603 22u*1
0402 10u*2
0402 10u*1 DY

0402 12p*3
0402 2.2p*3
0402 10u*16
0402 10u*6 DY
0603 22u*2 DY

1D05V_VCCST

1D05V_VCCSTG

1D05V_VCCSTG_FPGM

618429_TGL_H_PDG_Rev1p0 .CPU PI_PDBOM

TGL-H soldered down (Customer recommendation for POR stackup) (8 Layers BOB)			
	Primary	Secondary	Comment
VDD2		1x 10uF 0402	Place as close as possible to the inner row of VDDQ BGAs
		2x 0402 Placeholer	
		2x 22uF 0603	

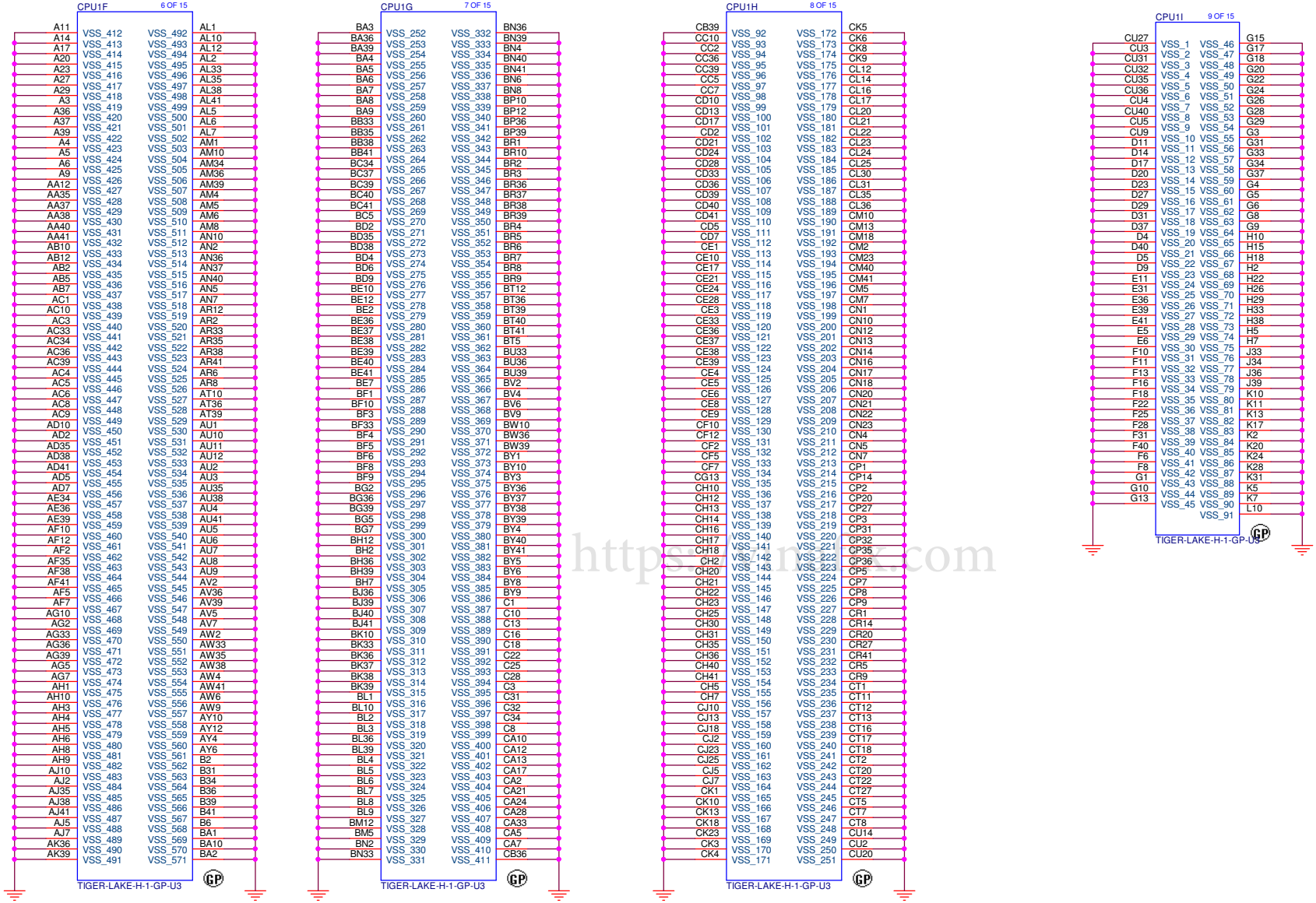
TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCCIN_AUX/VCCST/VCCSTG/VCCDD2/Others)

Size: A3 | Document Number: Cyborg_TGL-H RTX | Rev: X01

Date: Friday, November 20, 2020 | Sheet 8 of 106



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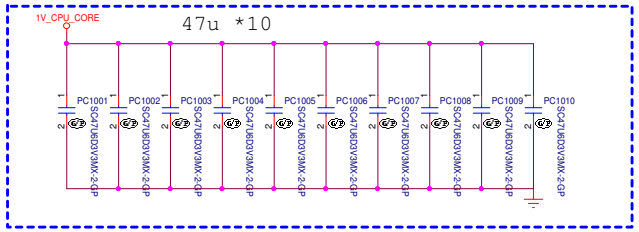
TGL-H

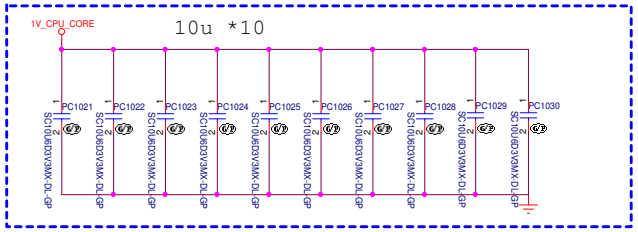
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

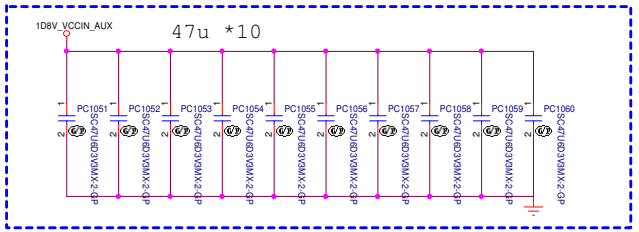
Title: CPU (VSS)

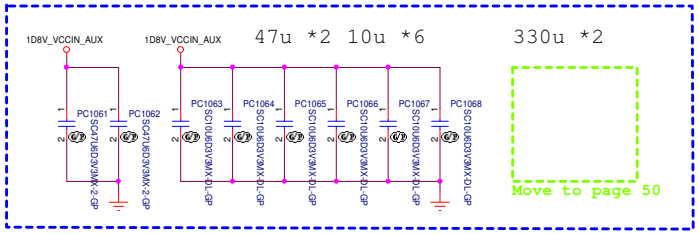
Size	Document Number	Rev
A3	Cyborg_TGL-H RTX	X01

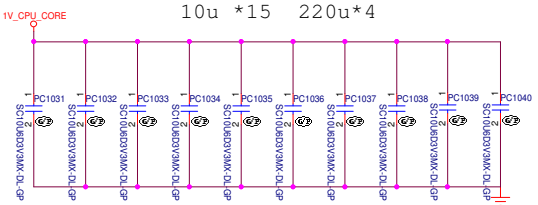
Date: Friday, November 20, 2020 Sheet 9 of 106

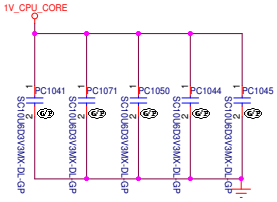


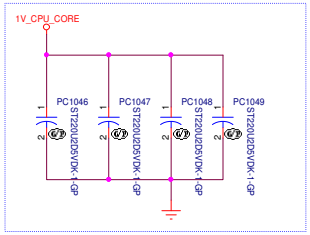






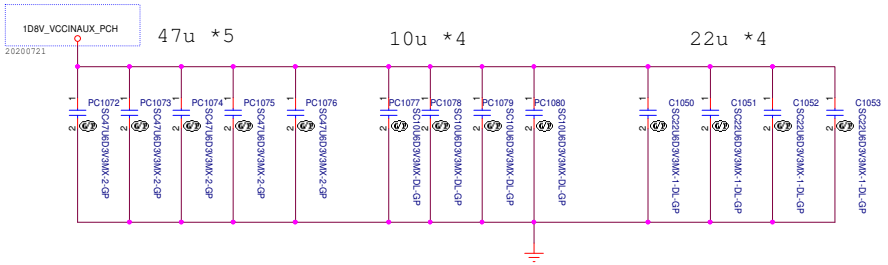


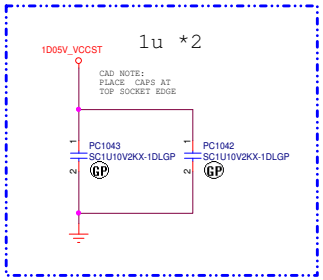


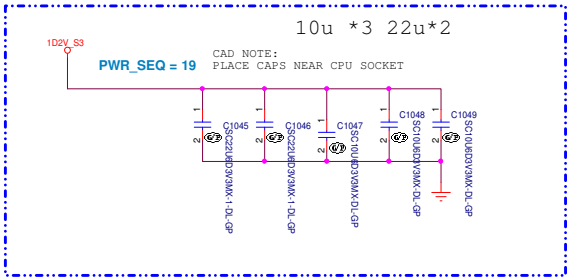


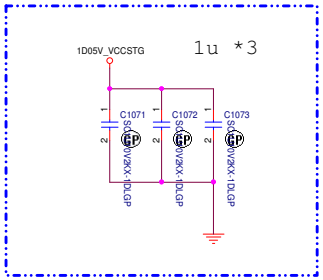
20200708
Change to 2.5V 7343H40

	Primary	Secondary	Comment
VCCIN_AUX_PCH	5x 47uF 0805 1x 47uF 0603 1x 22uF 0603 4x 10uF 0402		3 x 0805 47uF @ near PCH BGA 2 x 0805 47uF @ near VR









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TGL-H

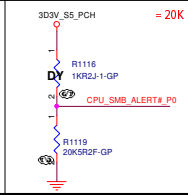
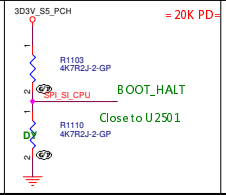
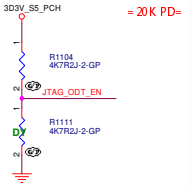
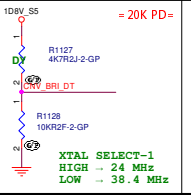
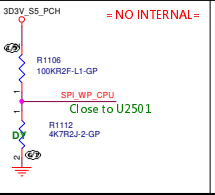
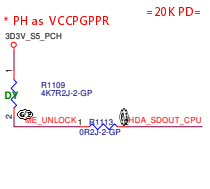
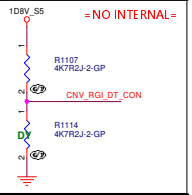
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

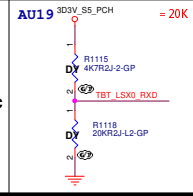
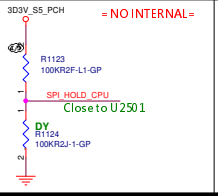
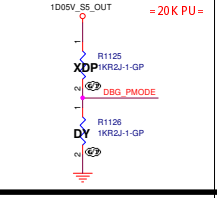
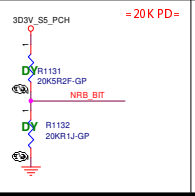
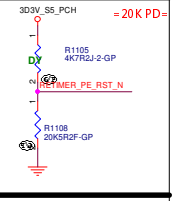
Title: CPU (CORE Power Cap1)

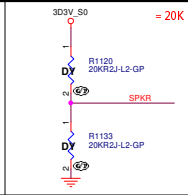
Size	Document Number	Rev
C	Cyborg_TGL-H RTX	X01

Date: Friday, November 20, 2020 Sheet 10 of 106

18,24,25,91 SPI_SI_CPU
18,24,25 SPI_WP_CPU
18,24,25 SPI_HOLD_CPU
21,61 CNV_RGI_DT_CON
21 JTAG_ODT_EN
21,24 HDA_SDOUT_CPU
20 DBG_PMODE
20,71 TBT_LSX0_RXD
20 CPU_SMB_ALERT#_P0
16,71 RETIMER_PE_RST_N
21 CNV_BRI_DT
20 NRB_BIT
20,24,27 SPKR

GPIO	GPP_C5/SML0ALERT#	SPI0_MOSI	GPP_H15 / SML3ALERT#	GPP_J2/ CNV_BRI_DT	SPI_IO_2	GPP_R2 / HDA_SDO	GPP_J4/ CNV_RGI_DT
Schematic							
High	Disable eSPI	Enable No Reboot mode	JTAG ODT is Enable	24 MHz		Disable Flash Descriptor Security	INTEGRATED CNVI DISABLE
Low	Enable eSPI = default=	Disable No Reboot mode	JTAG ODT is Disable	38.4 MHz = default=		Enable Flash Descriptor security measures	INTEGRATED CNVI ENABLE

GPIO	GPP_G13/ TBT_LSX0_VCC config				SPI0_IO3	DBG_PMODE	GPP_B18/GSPI0_MOSI	GPD7
Schematic	AU19 							
High	DDP4 I2C/TBT_LSX0/BBSB_LSO pins at 3.3V	3.3V	3.3V	3.3V		DFXTESTMODE DISABLED (DEFAULT)		
Low	DDP4 I2C/TBT_LSX0/BBSB_LSO pins at 1.8V	1.8V	1.8V	1.8V	Enable	DFXTESTMODE ENABLED		

GPIO	GPP_B14 / SPKR	GPP_C2/SMBALERT#	GPP_B23/SML1ALERT#	GPP_H12/SML2ALERT#	GPP_H18/SML4ALERT#	GPP_B22/GSPI1_MOSI		
Schematic			= 20K PD=	= 20K PD=	= 20K PD=	= 20K PD=		
High	TOP SWAP ENABLED	TLS CONFIDENTIALITY ENABLE						
Low	DISABLED	TLS CONFIDENTIALITY DISABLE						

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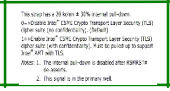
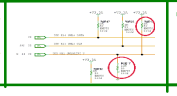
Original Ref.

GPP_C5	SPI0_MOSI	GPP_H15 / SML3ALERT#	GPP_J2/ CNV_BRI_DT	SPI0_IO2	GPP_R2 / HDA_SDO	GPP_J4/ CNV_RGI_DT	GPP_G13/ TBT_LSX0_VCC config		
ESPI LOW :ESPI IS DISABLED High :ESPI IS Enabled WEAK INTERNAL PD	External pull-up is required. Recommend 4.7 kohm pull up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	JTAG ODT DISABLE HIGH :JTAG ODT DISABLED LOW :JTAG ODT ENABLED	XTAL SELECT-1 HIGH -> 24 MHz LOW -> 38.4 MHz	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.		This strap does not have an internal pull-up or pull-down. A weak external pull-up is required. 0=>Integrated CNVi enabled. 1=>Integrated CNVi disabled. Note: When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down resistor will pull the strap low to enable CNVi interface.			

	SPI0_IO3	DBG_PMODE	GPP_B18/ GSPI0_MOSI	GPD7	GPP_B14 / SPKR	GPP_C2/ SMBALERT#	GPP_B23/ SML1ALERT#	GPP_H12/ SML2ALERT#	GPP_B22/ GSPI1_MOSI
	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	This strap has a 20 kohm ± 30% internal pull-up. This strap should sample high. There should NOT be any on-board device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-up is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.	No REBOOT HIGH :NO REBOOT LOW :REBOOT ENABLED WEAK INTERNAL PD	This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-down is disabled after DSW_PWROK is high. 2. This signal is in the DSW well.					

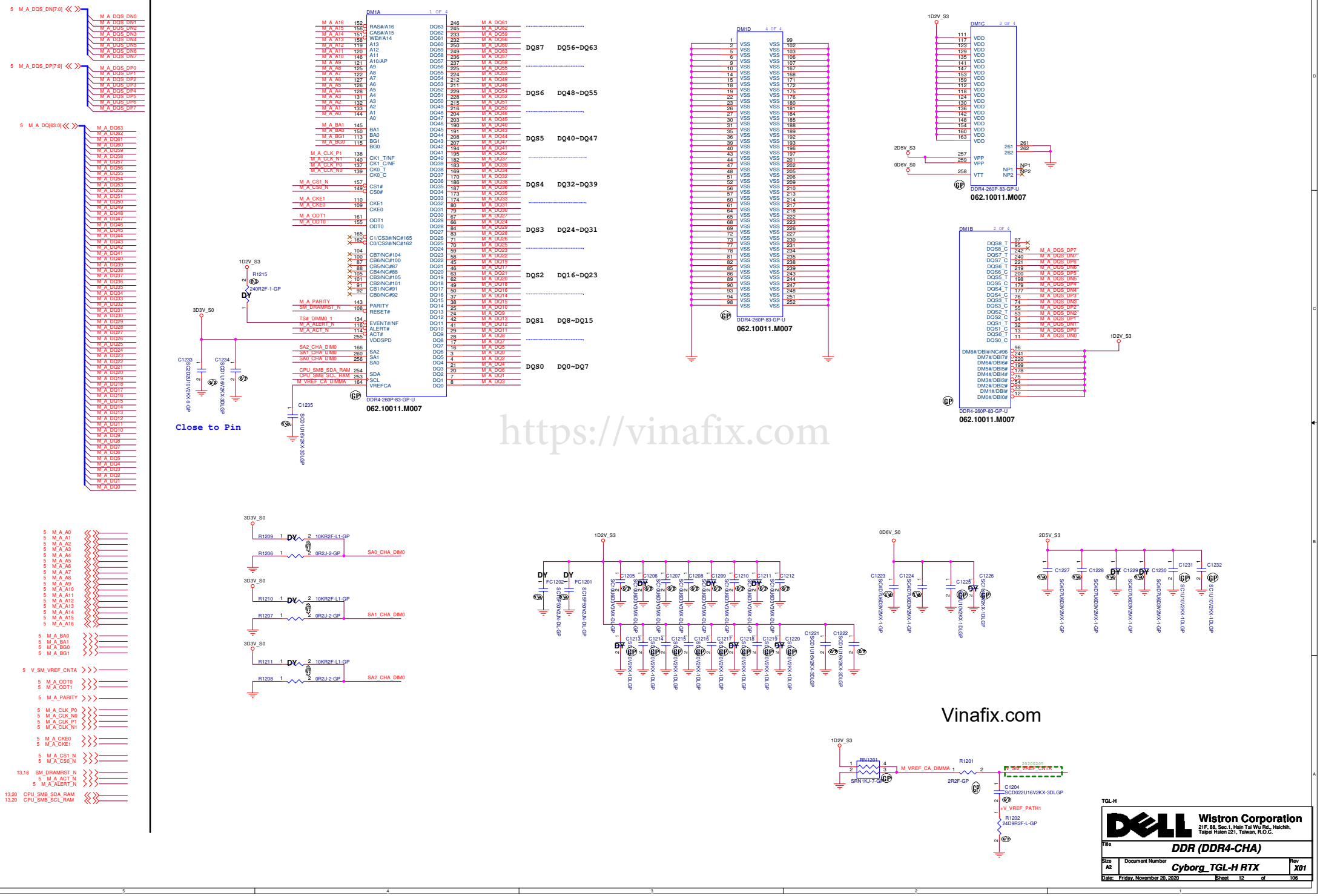
TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size	Document Number	Rev
A2	Cyborg_TGL-H RTX	X01

Date: Friday, November 20, 2020 Sheet 11 of 106


DM1A
DM1B
DM1C
DM1D
DDR4-260P-83-GP-U
062.10011.M007
DQS7 DQ56~DQ63
DQS6 DQ48~DQ55
DQS5 DQ40~DQ47
DQS4 DQ32~DQ39
DQS3 DQ24~DQ31
DQS2 DQ16~DQ23
DQS1 DQ8~DQ15
DQS0 DQ0~DQ7
Close to Pin
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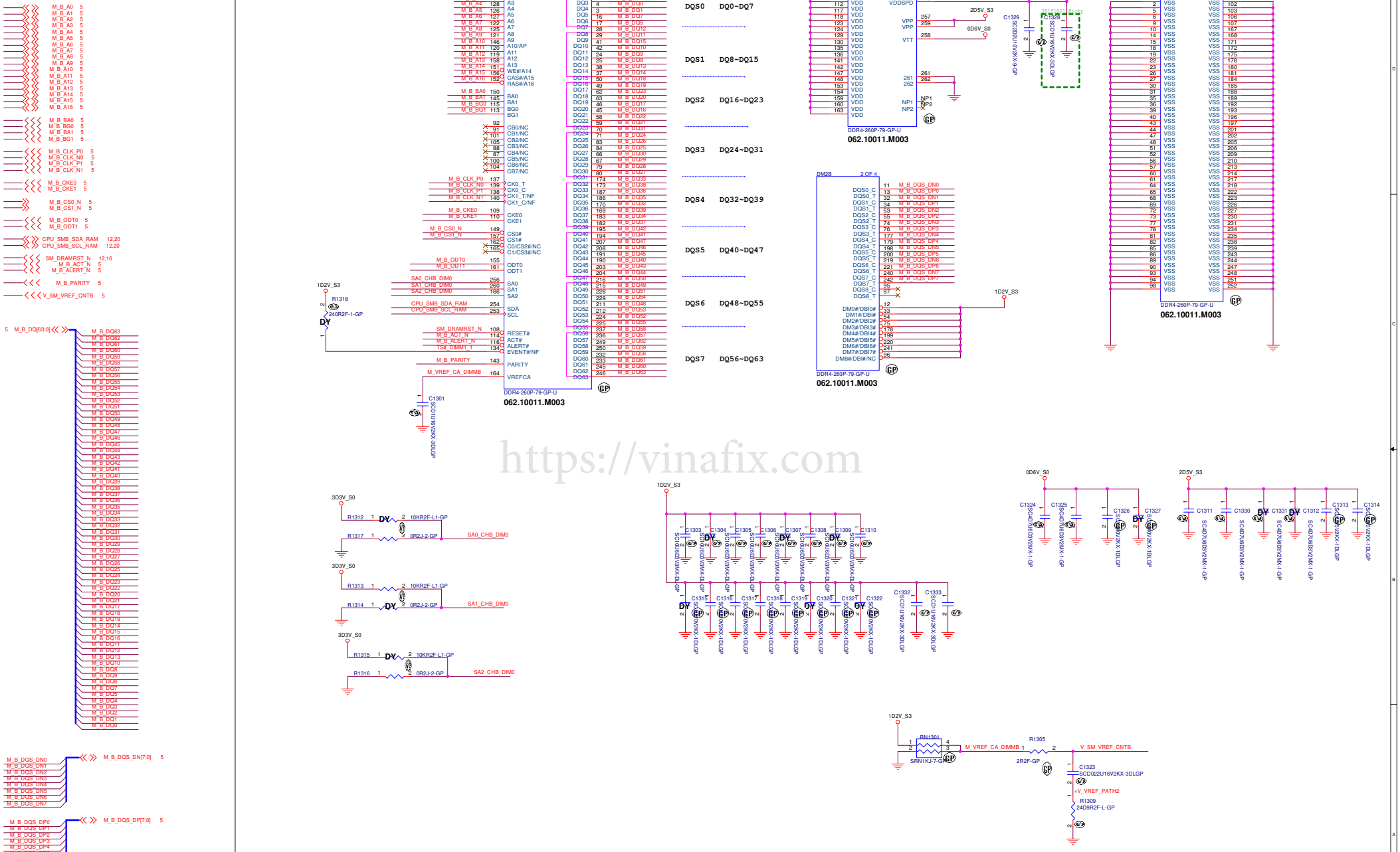
Vinafix.com
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR (DDR4-CHA)
Cyborg_TGL-H RTX
X01
Friday, November 20, 2020



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TGL-H

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DDR (DDR4-CHB)		
Size: A2	Document Number: Cyborg_TGL-H RTX	Rev: X01
Date: Friday, November 20, 2020	Sheet 13 of 106	

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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (RSVD) (DDR4-CHA1)

Size	Document Number	Rev
A3	Cyborg_TGL-H RTX	X01

Date: Friday, November 20, 2020 Sheet 14 of 106

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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

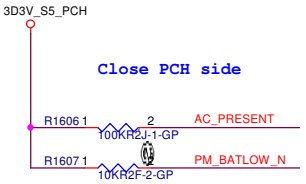
Title: DDR (RSVD) (DDR4-CHB1)

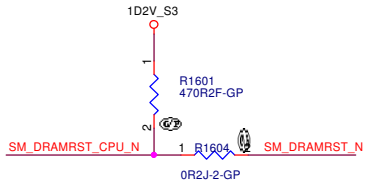
Size	Document Number	Rev
A3	Cyborg_TGL-H RTX	X01

Date: Friday, November 20, 2020 Sheet 15 of 106

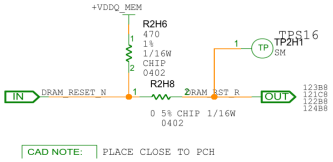
618429_TGL_H_SchChk_Rev1p0 P.61

BATLOW#/GPD0	10 kΩ to 100 kΩ pull-up to DSW well.	Pull-up required even if not implemented.
ACPRESENT/ GPD1	100 kΩ pull-up to DSW rail.	Point-to-point connection between PCH and EC. To indicate that system is powered by AC. This is a required signal for platforms with or without M3 support. A lower value pull- down is OK here on this signal because it only draws power when the brick is present (no impact to battery life). Refer to Tiger Lake PCH-H Platform Controller Hub External Design Specification (EDS) for details.





618697_TGL_H_DDR4_SCH_REV1P1 P.124



PCH_GPP	TGL
GPP_A	Multi
GPP_B	3.3 V
GPP_C	3.3 V
GPP_D	1.8 V
GPP_E	3.3 V
GPP_F	3.3 V
GPP_G	Multi
GPP_H	3.3 V
GPP_I	3.3 V
GPP_J	1.8 V only
GPP_K	3.3 V
GPP_R	3.3 V
GPP_S	1.8 V only
GPD	3.3 V only

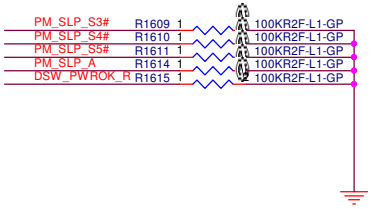
618429_TGL_H_PDG_Rev1p0 P.147.148

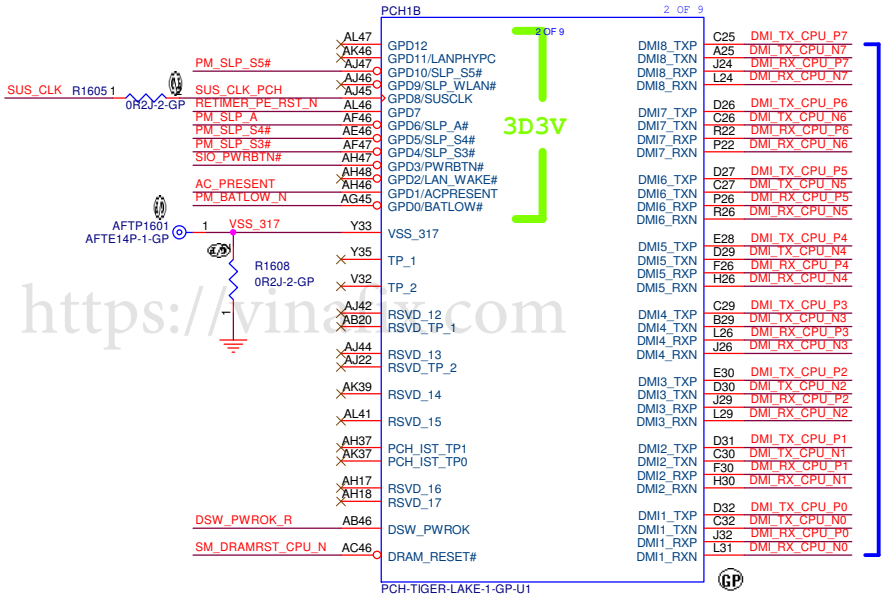
Table 68. Signals Required Pull-Down Resistor

Signal Name	Pull-down Resistor Implementation		Note
	3.3V Signaling Mode	1.8V Signaling Mode	
GPD4 / SLP_S3# GPD5 / SLP_S4# GPD6 / SLP_A# GPD9 / SLP_WLAN#	100K	N/A	Pull-down resistor is required
GPP_J1 / CPU_C10_GATE#	N/A	75K	
SLP_SUS# SLP_LAN#	100K	N/A	
SPI0_CLK	100K	75K	

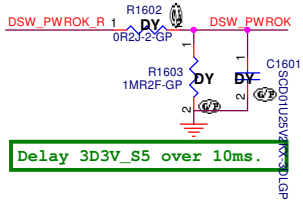
Table 69. Signals Recommended with pull-down Resistor Sites

Signal Name	Pull-down Resistor Implementation	Note
GPD10 / SLP_S5# GPP_A6 / ESPI_RESET	Pull-down resistor site	Site for pull-down resistor only.
GPP_B13 / PLTRST# HDA_BCLK / I2S0_SCLK HDA_RST# / I2S1_SCLK I2S1_SFRM / SNDW2_CLK		





DMI



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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DMI/PM/FIVR)

Size: A3 | Document Number: Cyborg_TGL-H RTX | Rev: X01

Date: Friday, November 20, 2020 | Sheet 16 of 106

WLAN

61 WLAN_PCIE_TX_P
61 WLAN_PCIE_TX_N
61 WLAN_PCIE_RX_P
61 WLAN_PCIE_RX_N

SSD2

63 SSD2_PCIE_RX_N1
63 SSD2_PCIE_RX_P1
63 SSD2_PCIE_TX_N1
63 SSD2_PCIE_TX_P1

63 SSD2_PCIE_RX_N2
63 SSD2_PCIE_RX_P2
63 SSD2_PCIE_TX_N2
63 SSD2_PCIE_TX_P2

63 SSD2_PCIE_RX_N3
63 SSD2_PCIE_RX_P3
63 SSD2_PCIE_TX_N3
63 SSD2_PCIE_TX_P3

63 SSD2_SATA_RX_N4
63 SSD2_SATA_RX_P4
63 SSD2_SATA_TX_N4
63 SSD2_SATA_TX_P4

40,50,52 PWR_VCCAUX_PCH_PG

24,53 PM_SLP_SUS#
24 EC_PCH_SPI_EN
64 PM_RSMRST_N
16,27,40,55,57 PM_SLP_S3#
6 CPU_JTAG_PRDY_N
6 CPU_JTAG_PREQ_N
6 CPU_SYNC
6 CPU_DOWN
6 CPU_PLT_RST_N
6,24 PECI_PCH
44,46 PCH_PWROK
16 DSW_PWROK_R

16 DSW_PWROK
16 AC_PRESENT
43,44 ACOK_IN_M
24 PCH_DPWROK
24 PCH_RSMRST#
25,40,45 3V_5V_POK

Dell_CY21_CSB_HSIO_Port_Assignment_Rev0.1_2020-04-07_Cyborg-H

HSIO Type and Lane		Cyborg-H
DMI 7		DMI x 8
PCIe Gen3 #9	GbE	1st PCH M.2 SSD <Gen3>
PCIe Gen3 #10		
PCIe Gen3 #11	SATA 0a	
PCIe Gen3 #12	SATA 1a / GbE	
PCIe Gen3 #15	SATA2	WLAN M.2

RTC_AUX_S5
R1703 20KR2J-L2-GP
RTC_RST_N
G1701 GAP-OPEN
C1703 SC1U10V2KX-1GP

3D3V_AUX_S5
R1715 100KR2J-1-GP
R1708 10KR2J-3-GP
PM_RSMRST
Q1701 2N7002KDW-1-GP
PM_RSMRST_N
R1709 1KR2J-1-GP
PCH_RSMRST#
3V_5V_POK_C
D1705 RB520S30-GP
3V_5V_POK
83.R2003.A8M
2ND = 83.52030.008F
D1706 RB520S30-GP
PWR_VCCAUX_PCH_PG
R1711 100KR2J-1-GP

Need Check Sequence

D1701 RB520S30-GP
83.R2003.A8M
2ND = 083.52030.008F
ACOK_IN_M
3D3V_AUX_S5
Q1702 2N7002KDW-1-GP
75.27002.F7C
AC_PRESENT
R1704 100KR2J-1-GP
PM_RSMRST#_M
PM_RSMRST#_R
R1705 0R2J-2-GP
PM_RSMRST_N
2nd = 075.67002.007C
3rd = 075.063D1.007C

Reserve by NON DS3 function 20150413

SCD1U16V2KX-3DLGP
C1714
3D3V_S5
U1703 G3904M41U-GP
VDD
PWROK
PWRGD
PCHRST
NC#
PCHPOK
EC_EN
GND
3D3V_S5_U
R1771 0R1J-GP
3D3V_S5_R
3V_5V_PWRGD_U
R1772 0R1J-GP
3V_5V_POK
PCH_RSMRST#
R1773 0R1J-GP
PCH_RSMRST#_U
PCH_DPWROK
R1775 0R1J-GP
PCH_DPWROK_R
EC_PCH_SPI_EN
R1774 0R1J-GP
EC_PCH_SPI_EN_R
074.03904.0053

PCH1E
5 OF 9
CPU_JTAG_PRDY_N AF3
CPU_JTAG_PREQ_N AF4
CPU_SYNC AH4
CPU_DOWN AH2
CPU_PLT_RST_N AE3
PECI_PCH AH3
PRDY#
PREQ#
PM_SYNC
PM_DOWN
PLTRST_CPU#
PECI
V29 RSVD_10
V28 RSVD_11
H45 PCIE24_TXP
G45 PCIE24_TXN
T42 PCIE24_RXP
T43 PCIE24_RXN
J46 PCIE23_TXP
J47 PCIE23_TXN
P35 PCIE23_RXP
P37 PCIE23_RXN
G47 PCIE22_TXP
F47 PCIE22_TXN
H39 PCIE22_RXP
P41 PCIE22_RXN
E48 PCIE21_TXP
E49 PCIE21_TXN
N43 PCIE21_RXP
N42 PCIE21_RXN
B44 PCIE20_TXP/SATA7_TXP
A44 PCIE20_TXN/SATA7_TXN
M37 PCIE20_RXP/SATA7_RXP
M35 PCIE20_RXN/SATA7_RXN
D43 PCIE19_TXP/SATA6_TXP
C43 PCIE19_TXN/SATA6_TXN
L41 PCIE19_RXP/SATA6_RXP
N39 PCIE19_RXN/SATA6_RXN
C42 PCIE18_TXP/SATA5_TXP
B42 PCIE18_TXN/SATA5_TXN
L42 PCIE18_RXP/SATA5_RXP
K43 PCIE18_RXN/SATA5_RXN
E41 PCIE17_TXP/SATA4_TXP
D42 PCIE17_TXN/SATA4_TXN
G43 PCIE17_RXP/SATA4_RXP
F44 PCIE17_RXN/SATA4_RXN
C40 PCIE16_TXP/SATA3_TXP
D40 PCIE16_TXN/SATA3_TXN
C47 PCIE16_RXP/SATA3_RXP
D46 PCIE16_RXN/SATA3_RXN
D39 PCIE15_TXP/SATA_2_TXP
C39 PCIE15_TXN/SATA2_TXN
C46 PCIE15_RXP/SATA2_RXP
D45 PCIE15_RXN/SATA2_RXN
E38 PCIE14_TXP/SATA1B_TXP
D38 PCIE14_TXN/SATA1B_TXN
H42 PCIE14_RXP/SATA1B_RXP
J41 PCIE14_RXN/SATA1B_RXN
B37 PCIE13_TXP/SATA0B_TXP
C38 PCIE13_TXN/SATA0B_TXN
G39 PCIE13_RXP/SATA0B_RXP
H38 PCIE13_RXN/SATA0B_RXN
PCH-TIGER-LAKE-1-GP-U1
ZZ.00PCH.021

PCIE12_TXP/SATA1A_TXP C36 SSD2_SATA_TX_P4
PCIE12_TXN/SATA1A_TXN D36 SSD2_SATA_TX_N4
PCIE12_RXP/SATA1A_RXP L36 SSD2_SATA_RX_P4
PCIE12_RXN/SATA1A_RXN J37 SSD2_SATA_RX_N4
PCIE11_TXP/SATA0A_TXP D35 SSD2_PCIE_TX_P3
PCIE11_TXN/SATA0A_TXN C35 SSD2_PCIE_TX_N3
PCIE11_RXP/SATA0A_RXP G36 SSD2_PCIE_RX_P3
PCIE11_RXN/SATA0A_RXN H35 SSD2_PCIE_RX_N3
PCIE10_TXP D34 SSD2_PCIE_TX_P2
PCIE10_TXN E34 SSD2_PCIE_TX_N2
PCIE10_RXP J35 SSD2_PCIE_RX_P2
PCIE10_RXN L34 SSD2_PCIE_RX_N2
PCIE9_TXP C33 SSD2_PCIE_TX_P1
PCIE9_TXN B33 SSD2_PCIE_TX_N1
PCIE9_RXP G33 SSD2_PCIE_RX_P1
PCIE9_RXN H33 SSD2_PCIE_RX_N1
M.2 SSD2
PCIE8_TXP B21
PCIE8_TXN A22
PCIE8_RXP F24
PCIE8_RXN H24
PCIE7_TXP C23
PCIE7_TXN D23
PCIE7_RXP P19
PCIE7_RXN R19
PCIE6_TXP E20
PCIE6_TXN D20
PCIE6_RXP J21
PCIE6_RXN L21
PCIE5_TXP D21
PCIE5_TXN C21
PCIE5_RXP F20
PCIE5_RXN H20
PCIE4_TXP/USB31_10_TXP D19
PCIE4_TXN/USB31_10_TXN C20
PCIE4_RXP/USB31_10_RXP P17
PCIE4_RXN/USB31_10_RXN R17
PCIE3_TXP/USB31_9_TXP E17
PCIE3_TXN/USB31_9_TXN D17
PCIE3_RXP/USB31_9_RXP H17
PCIE3_RXN/USB31_9_RXN G17
PCIE2_TXP/USB31_8_TXP C18
PCIE2_TXN/USB31_8_TXN D18
PCIE2_RXP/USB31_8_RXP J18
PCIE2_RXN/USB31_8_RXN L19
PCIE1_TXP/USB31_7_TXP C17
PCIE1_TXN/USB31_7_TXN B17
PCIE1_RXP/USB31_7_RXP J15
PCIE1_RXN/USB31_7_RXN L16
PCH_PWROK AB47 PM_PCH_PWROK
RTCRST# AM45 RTC_RST_N
RSMRST# AA45 PM_RSMRST_N
RTCX2 AM48 XTL_32K_X2_CPU
RTCX1 AM46 XTL_32K_X1_CPU

WLAN
WLAN_PCIE_TX_P D39
WLAN_PCIE_TX_N C39
WLAN_PCIE_RX_P C46
WLAN_PCIE_RX_N D45

3D3V_S0
R1714 10KR2J-3-GP
PCH_PWROK
R1777 1 2 0R1J-GP
PM_PCH_PWROK
PM_SLP_S3#
D1704 RB751V-40H-GP
R1117 100KR2F-L1-GP
83.R2004.G8F

XTL_32K_X1_CPU
XTL_32K_X2_CPU
R1702 10MR2J-3-GP
X1701 XTAL-32D768KHZ-98-GP
C1702 SC18P50V2JN-1-GP
082.30003.0301
C1701 SC18P50V2JN-1-GP

618429_TGL_H_SchChk_Rev1p0 P.60

Power rail / Signal Name	System Pull-up / Pull-down	Schematics Notes
PCH_PWROK	10 kohm to 100 kohm pull-down to GND.	When asserted, PWROK is an indication to the PCH that all of its core power rails have been stable. The platform may drive asynchronously PCH_PWROK high any time after it has met all the required sequencing timings called out in the sequencing section of this Design Guide. When PWROK is negated, the PCH asserts PLTRST#. IMVP_VR_READY AND'd with IMVP_VR_ON generate PCH_PWROK. NOTE: If this signal is driven from an open drain source/ buffer the pull-up resistance should be in range 1/10th of pull-down resistance to ensure the voltage is sufficiently high enough to be seen as logic high by the platform. NOTE: The pulldown is not needed if the source of this signal can guarantee this signal is in proper state for G3 through S0.

Power on sequence for G3 sharing

3D3V_S5
3D3V_S5_PCH
300KR2F-GP
R1720 1
3D3V_S5_PCH_R
R1721 1
3D3V_S5_R
100KR2J-1-GP
U1701 74LVC1G08GW-1-GP
C1713 SC1U10V2KX-2GP
73.01G08.L04
2nd = 073.7SZ08.000G
3rd = 073.01G08.IHG
4th = 73.7SZ08.DAH
DSW_PWROK_R
R1776 0R1J-GP
DY
Need fine tune
C1712 SC1U16V2KX-3DLGP
R1734 0R2J-2-GP
Q1703 2N7002KDW-1-GP
75.27002.F7C
Q1703_2_3
R1735 100KR2J-1-GP
R1736 10KR2F-2-GP
R1740 1MR2F-GP
DSW_PWROK
PM_SLP_SUS#
R1741 0R1J-GP
DSW_PWROK_EN
U1704 74LVC1G08GW-1-GP
73.01G08.L04
2nd = 073.7SZ08.000G
3rd = 073.01G08.IHG
4th = 73.7SZ08.DAH
PCH_RSMRST#
U1702
PM_RSMRST_N
D1703 RB520S30-GP
PCH_DPWROK
83.R2003.A8M
2nd = 083.52030.008F
D1702 RB520S30-GP
3D3V_S5_R
PCH_DPWROK
83.R2003.A8M
2nd = 083.52030.008F

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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCIE/SATA/RTC)
Size: A2
Document Number: Cyborg_TGL-H RTX
Rev: X01
Date: Friday, November 20, 2020
Sheet 17 of 106

USB2

72 USB1_USB20_P
72 USB1_USB20_N

35 USB2_USB20_P
35 USB2_USB20_N

55 CCD_USB20_P
55 CCD_USB20_N

61 BT_USB20_P
61 BT_USB20_N

66 USB3_USB20_P
66 USB3_USB20_N

66 CARD1_USB20_P
66 CARD1_USB20_N

66 FP1_USB20_P
66 FP1_USB20_N
20200206

35 USB2_USB30_TX_N
35 USB2_USB30_TX_P
35 USB2_USB30_RX_N
35 USB2_USB30_RX_P
20200207

Others

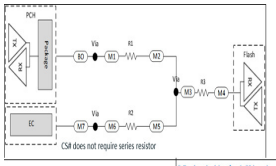
6 THERMTRIP_CPU_N
6 PCH_2_CPU_TRIGGER
6 CPU_2_PCH_TRIGGER
24,53 PM_SLP_SUS#

24,25,91 SPI_SO_CPU
11,24,25,91 SPI_SI_CPU
11,24,25 SPI_HOLD_CPU
11,24,25 SPI_WP_CPU
24,25 SPI_CS_ROM_N0
24,25 SPI_CS_ROM_N1
24,25,91 SPI_CLK_CPU
24 SYS_PWROK
91 SPI_CS_CPU_N2

66 USB3_USB30_TX_N
66 USB3_USB30_TX_P
66 USB3_USB30_RX_N
66 USB3_USB30_RX_P

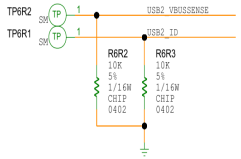
618697_TGL_H_DDR4_SCH_REV1P1 P.38

618429_TGL_H_PDG_Rev1p0 SPI0 Flash



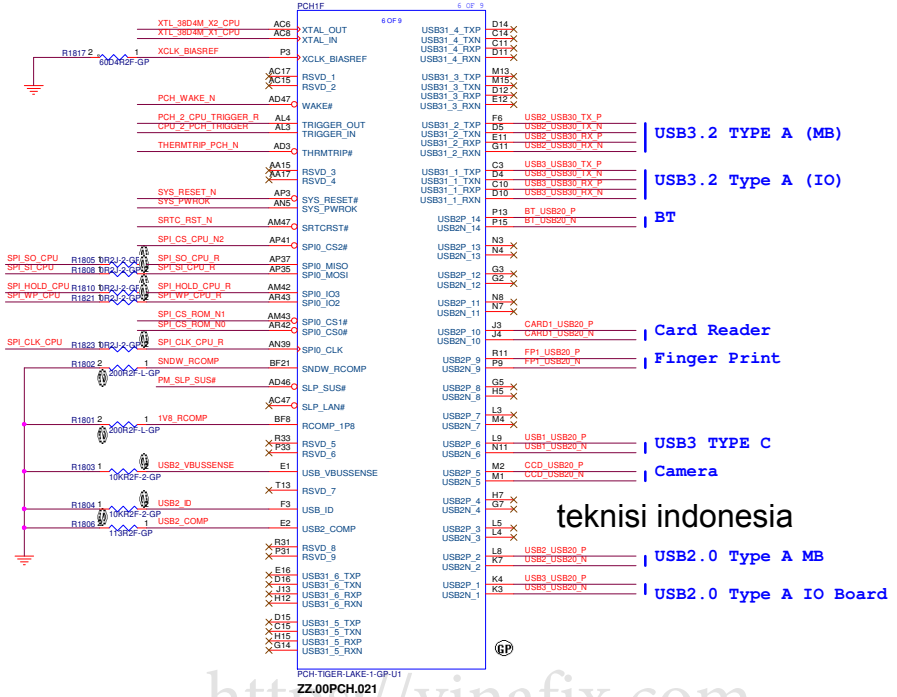
R1	0Ω placeholder for 1.8V and 15Ω for 3.3V To be placed on SPI0 CLK, SPI0 MISO, SPI0 MOSI, SPI0 IO 2 and SPI0 IO 3
R2	50Ω for 1.8V and 50Ω for 3.3V To be placed on SPI0 CLK, SPI0 MISO, SPI0 MOSI, SPI0 IO 2 and SPI0 IO 3
R3	33Ω for 1.8V and 50Ω for 3.3V To be placed on SPI0 CLK, SPI0 MISO, SPI0 MOSI, SPI0 IO 2 and SPI0 IO 3

618697_TGL_H_DDR4_SCH_REV1P1 P.38

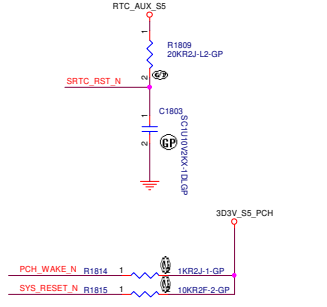


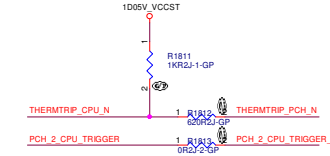
618429_TGL_H_PDG_Rev1p0 RCOMP

Pin Name	USB2_COMP	SNDW_RCOMP	RCOMP_1P8
Board Rterm (ohm)	113Ω±1% to GND	200Ω±1% to GND	200Ω±1% to GND
Board Rdc (ohm)	<0.5	<0.1	<0.1
Board Cap (pF)	N/A	N/A	N/A
Spacing for Breakout (um)	127	100	100
Spacing for Mainroute (um)	200		
DDR			
HDMI			
DP			
eDP			
DSI			
CSI			
Type-C			
PCIe4 x4			
PCIe4 x16			
DMI			
DPIP[0/1/2/3]			
ModPHY			
USB2	X		
GPIO_1.8V/3.3V			
SoundWire		X	
GPIO_1.8V			X
XTAL			
CNVi_DPHY			



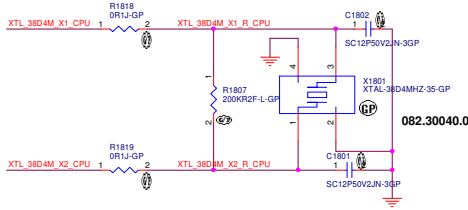
USB3.2 TYPE A (MB)
USB3.2 Type A (IO)
BT
Card Reader
Finger Print
USB3 TYPE C
Camera
USB2.0 Type A MB
USB2.0 Type A IO Board





Dell_CY21_CSB_HSIO_Port_Assignment_Rev0.1_2020-04-07_Cyborg-H

HSIO Type and Lane		Cyborg-H
USB3.2 Gen 1x1/2x1 #1	USB3.2 Gen 2x2 #1	USB3.2 Port (Right)
USB3.2 Gen 1x1/2x1 #2		USB3.2 Port (Left)
USB3.2 Gen 1x1/2x1 #3	USB3.2 Gen 2x2 #2	
USB3.2 Gen 1x1/2x1 #4		
DMI 7		DMI x 8
DMI 6		
DMI 5		
DMI 4		
DMI 3		
DMI 2		
DMI 1		
DMI 0		
PCIe Gen3 #9	GbE	1st PCH M.2 SSD <Gen3>
PCIe Gen3 #10		
PCIe Gen3 #11	SATA 0a	
PCIe Gen3 #12	SATA 1a / GbE	
PCIe Gen3 #15	SATA2	WLAN M.2
USB 2.0 P1		USB3.2 Port (Right)
USB 2.0 P2		USB3.2 Port (Left)
USB 2.0 P5		Camera
USB 2.0 P6		Type C USB2
USB 2.0 P9		Finger print
USB 2.0 P10		Card Reader
USB 2.0 P14		Bluetooth



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teknisi indonesia

TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (USB31/USB2/SPI/XTAL)

Size	Document Number	Rev
A2	Cyborg_TGL-H RTX	X01

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SSD

63 SSD2_CLK_CPU_P
63 SSD2_CLK_CPU_N

63 SSD_CLK_CPU_P
63 SSD_CLK_CPU_N

dGPU

76 GFX_CLK_CPU_P
76 GFX_CLK_CPU_N

WLAN

61 WLAN_CLK_CPU_P
61 WLAN_CLK_CPU_N

6,19 CPU_WAKE

CNVi

61 CNV_WT_DP1
61 CNV_WT_DN1
61 CNV_WT_DP0
61 CNV_WT_DN0
61 CNV_WT_CLKP
61 CNV_WT_CLKN

61 CNV_WR_DP1
61 CNV_WR_DN1
61 CNV_WR_DP0
61 CNV_WR_DN0
61 CNV_WR_CLKP
61 CNV_WR_CLKN

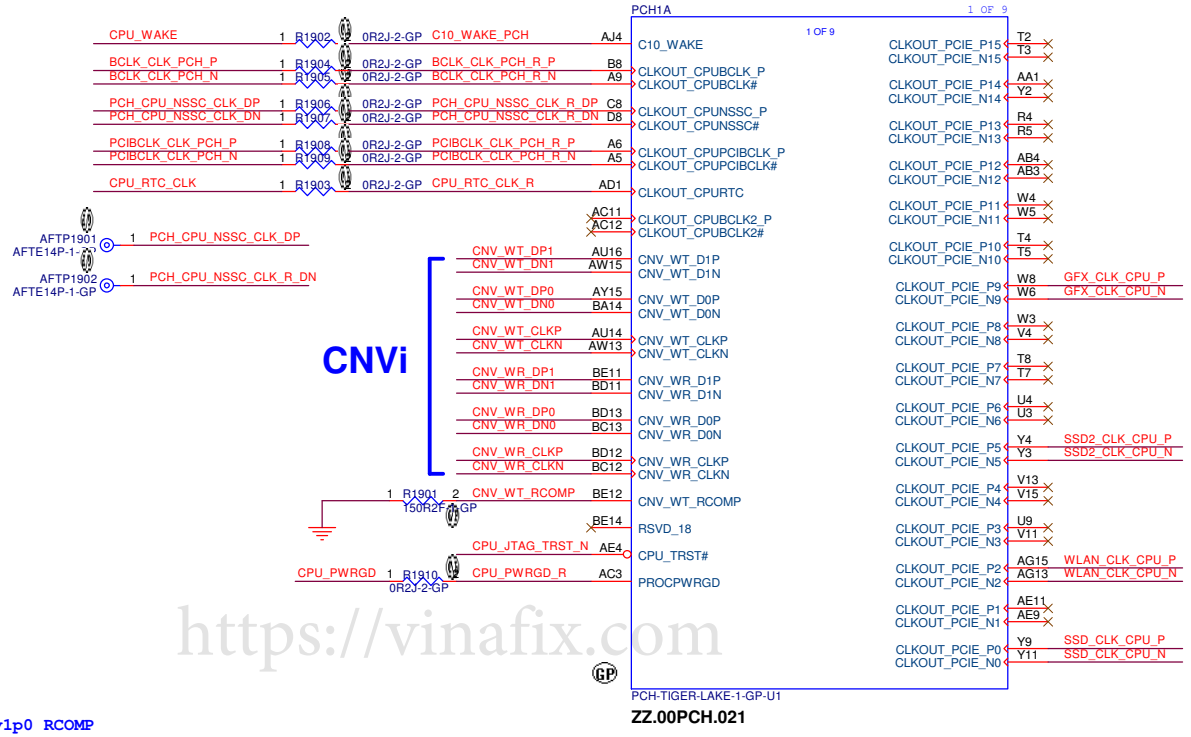
6 CPU_JTAG_TRST_N
6 CPU_PWRGD
6,19 CPU_WAKE

6 BCLK_CLK_PCH_P
6 BCLK_CLK_PCH_N

6 PCH_CPU_NSSC_CLK_DP
6 PCH_CPU_NSSC_CLK_DN

6 PCIBCLK_CLK_PCH_P
6 PCIBCLK_CLK_PCH_N

6 CPU_RTC_CLK



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618429_TGL_H_PDG_Rev1p0 RCOMP

Pin Name	CNVi_WT_RCOMP
Board Rterm (ohm)	150Ω±1% to GND
Board Rdc (ohm)	<0.5
Board Cap (pF)	N/A
Spacing for Breakout (um)	88
Spacing for Mainroute (um)	200
DDR	
HDMI	
DP	
eDP	
DSI	
CSI	
Type-C	
PCIe4 x4	
PCIe4 x16	
DMI	
DPIP[0/1/2/3]	
ModPHY	
USB2	
GPIO_1.8V/3.3V	
SoundWire	
GPIO_1.8V	
XTAL	
CNVi_DPHY	X

618429_TGL_H_PDG_Rev1p0 P.138

Table 65. Platform Clocks and Associated Signal Details and Descriptions

Signal Name	Type	SSC Capable	Description
CLKOUT_PCIE_P[15:0] CLKOUT_PCIE_N[15:0]	O	Yes	**PCI Express* Clock Output:** PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices. • CLKOUT_PCIE_P/N [15:0] = Can be used for PCIe* Gen1/2/3 support • CLKOUT_PCIE_P/N [9, 7, 4, 3, 0] = Must be used for PCIe* Gen4 support

TGL-H

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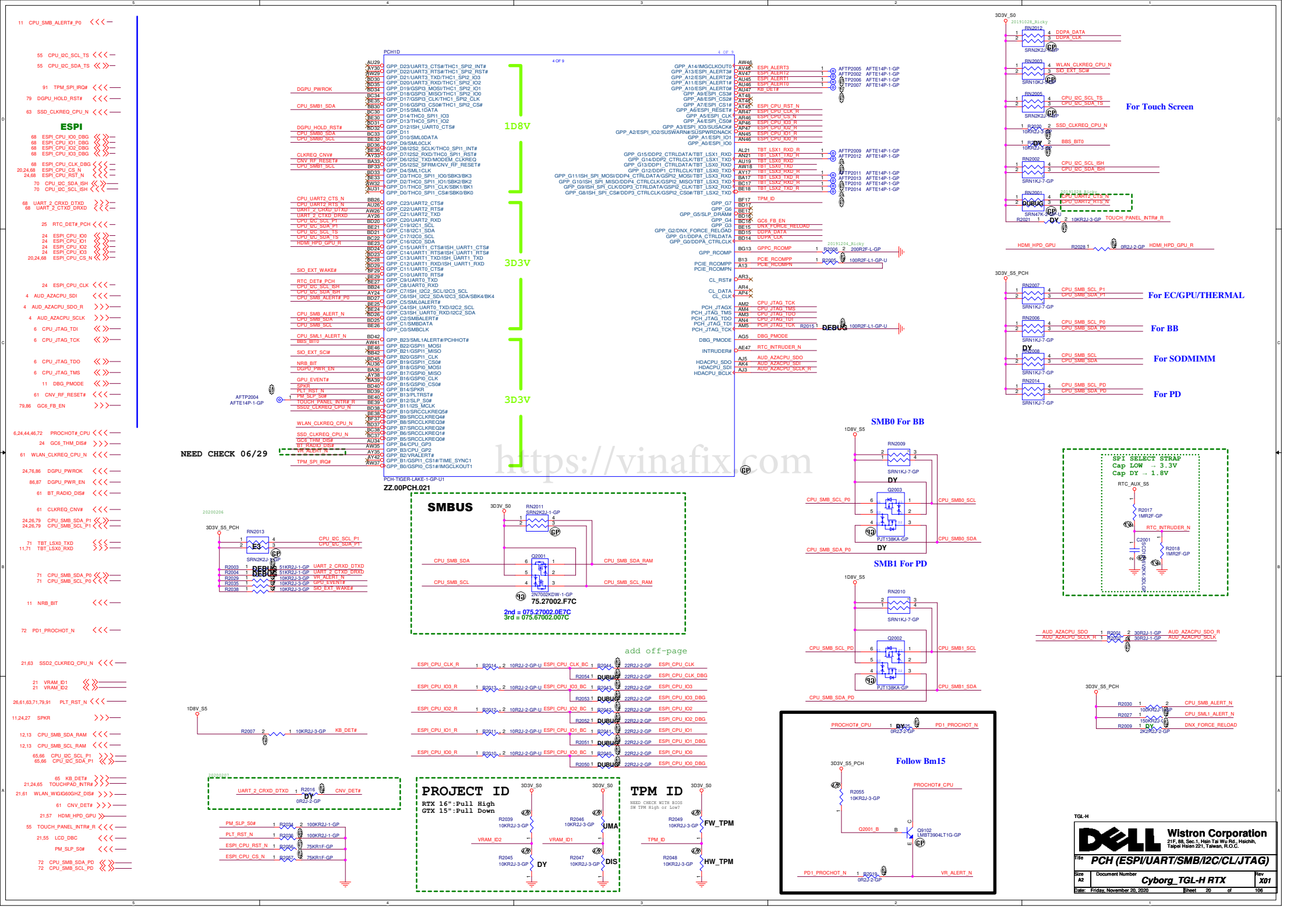
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (CLK/CNVi)

Size: A3 | Document Number: Cyborg_TGL-H RTX | Rev: X01

Date: Friday, November 20, 2020 | Sheet 19 of 106

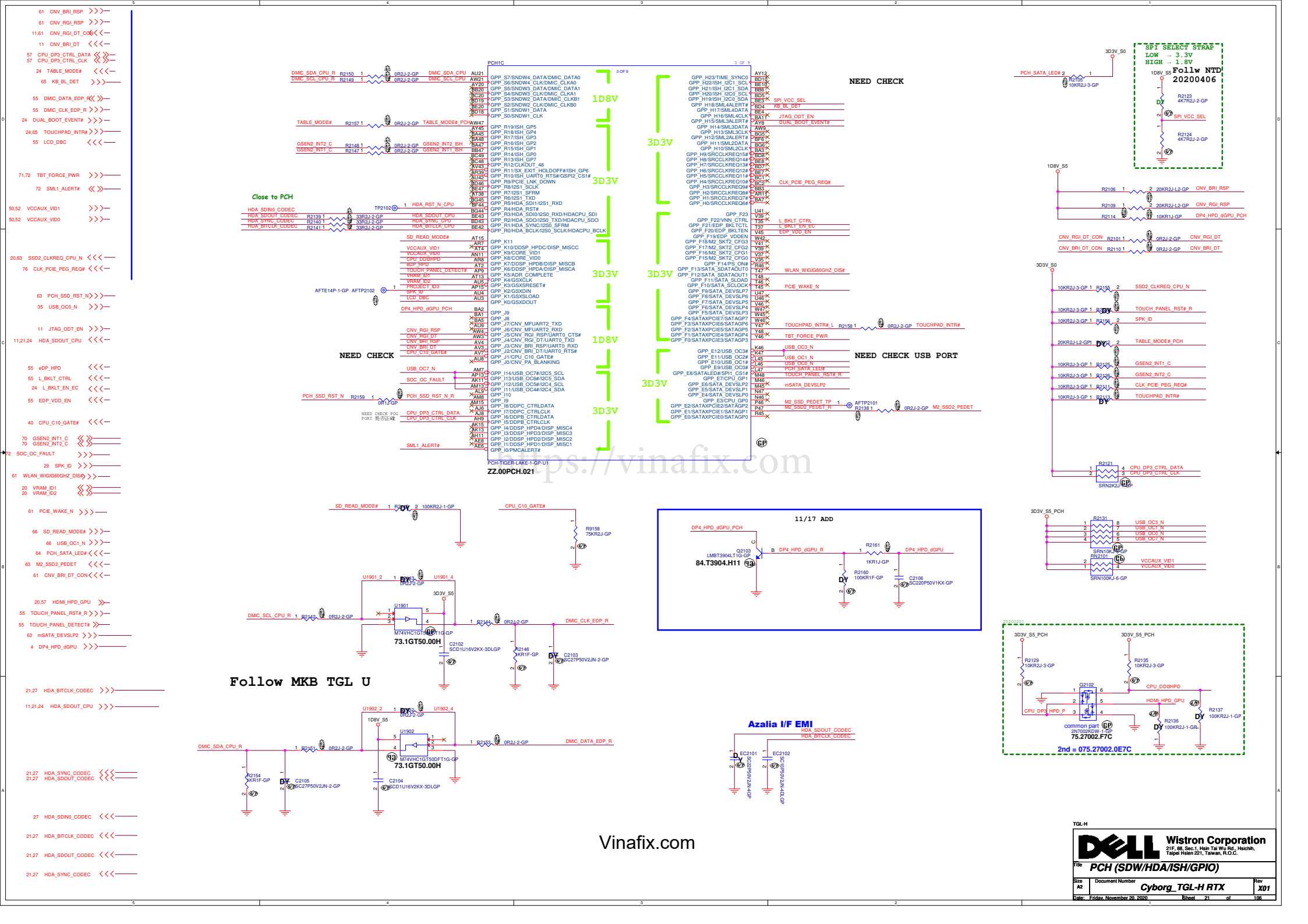


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (ESPI/UART/SMB/I2C/CL/JTAG)

Size	Document Number	Rev
A2	Cyborg_TGL-H RTX	X01

Date: Friday, November 20, 2020 Sheet 20 of 106


PCH1C
3 OF 9
GPP_S7/SNDW4_DATA/DMIC_DATA0
GPP_S6/SNDW4_CLK/DMIC_CLKA0
GPP_S5/SNDW3_DATA/DMIC_DATA1
GPP_S4/SNDW3_CLK/DMIC_CLKA1
GPP_S3/SNDW2_DATA/DMIC_CLKB1
GPP_S2/SNDW2_CLK/DMIC_CLKB0
GPP_S1/SNDW1_DATA
GPP_S0/SNDW1_CLK
GPP_R19/ISH_GP5
GPP_R18/ISH_GP4
GPP_R17/ISH_GP3
GPP_R16/ISH_GP2
GPP_R15/ISH_GP1
GPP_R14/ISH_GP0
GPP_R13/ISH_GP7
GPP_R12/CLKOUT_48
GPP_R11/ISX_EXIT_HOLDOFF#/ISH_GP6
GPP_R10/ISH_UART0_RTS#/GSPI2_CS1#
GPP_R9/PCIE_LNK_DOWN
GPP_R8/I2S1_SCLK
GPP_R7/I2S1_SFRM
GPP_R6/I2S1_TXD
GPP_R5/HDA_SDI1/I2S1_RXD
GPP_R4/HDA_RST#
GPP_R3/HDA_SDI0/I2S0_RXD/HDACPU_SDI
GPP_R2/HDA_SDO/I2S0_TXD/HDACPU_SDO
GPP_R1/HDA_SYNC/I2S0_SFRM
GPP_R0/HDA_BCLK/I2S0_SCLK/HDACPU_BCLK
GPP_K11
GPP_K10/DDSP_HPDC/DISP_MISCC
GPP_K9/CORE_VID1
GPP_K8/CORE_VID0
GPP_K7/DDSP_HPDB/DISP_MISCB
GPP_K6/DDSP_HPDA/DISP_MISCA
GPP_K5/ADR_COMPLETE
GPP_K4/GSXCLK
GPP_K3/GSXSRESET#
GPP_K2/GSXDIN
GPP_K1/GSXSLOAD
GPP_K0/GSXDOUT
GPP_J9
GPP_J8
GPP_J7/CNV_MFUART2_TXD
GPP_J6/CNV_MFUART2_RXD
GPP_J5/CNV_RGI_RSP/UART0_CTS#
GPP_J4/CNV_RGI_DT/UART0_TXD
GPP_J3/CNV_BRI_RSP/UART0_RXD
GPP_J2/CNV_BRI_DT/UART0_RTS#
GPP_J1/CPU_C10_GATE#
GPP_J0/CNV_PA_BLANKING
GPP_I14/USB_OC7#/I2C5_SCL
GPP_I13/USB_OC6#/I2C5_SDA
GPP_I12/USB_OC5#/I2C4_SCL
GPP_I11/USB_OC4#/I2C4_SDA
GPP_I10
GPP_I9
GPP_I8/DDPC_CTRLDATA
GPP_I7/DDPC_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I5/DDPB_CTRLCLK
GPP_I4/DDSP_HPD4/DISP_MISC4
GPP_I3/DDSP_HPD3/DISP_MISC3
GPP_I2/DDSP_HPD2/DISP_MISC2
GPP_I1/DDSP_HPD1/DISP_MISC1
GPP_I0/PMCALERT#
PCH-TIGER-LAKE-1-GP-U1
ZZ.00PCH.021
1D8V
3D3V
NEED CHECK
NEED CHECK USB PORT
Close to PCH
Follow MKB TGL U
73.1GT50.00H
84.T3904.H11
11/17 ADD
Azalia I/F EMI
SPI SELECT STRAP
LOW → 3.3V
HIGH → 1.8V
Follw NTD
20200406
2nd = 075.27002.0E7C
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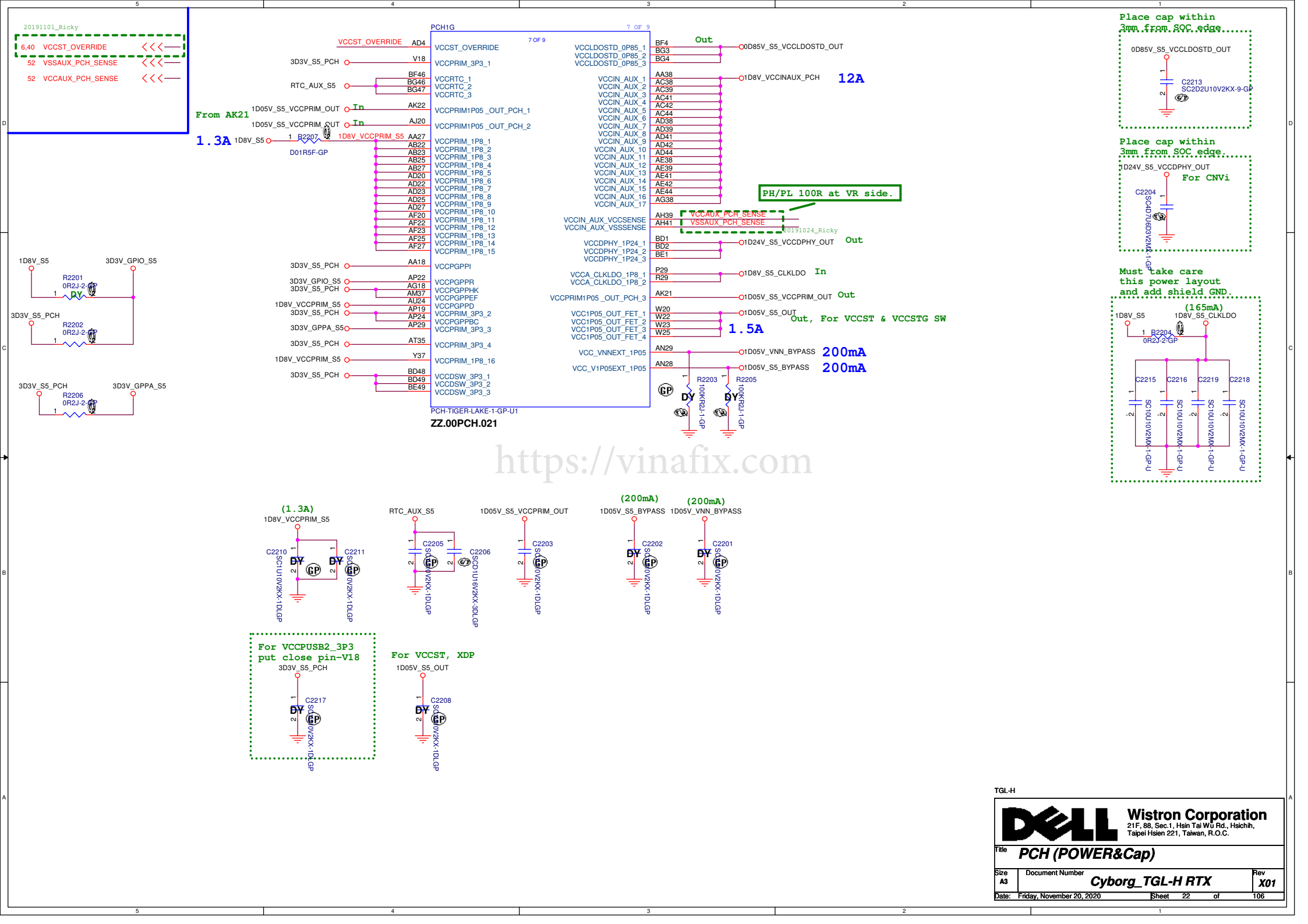
Wistron Corporation
PCH (SDW/HDA/ISH/GPIO)
Cyborg_TGL-H RTX
X01



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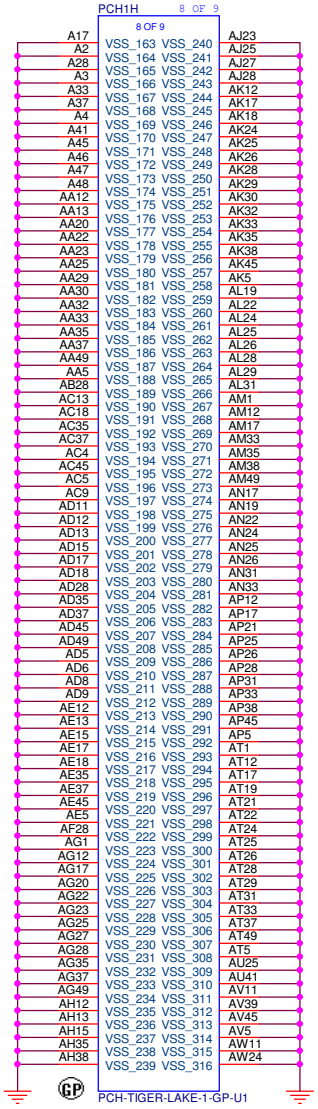
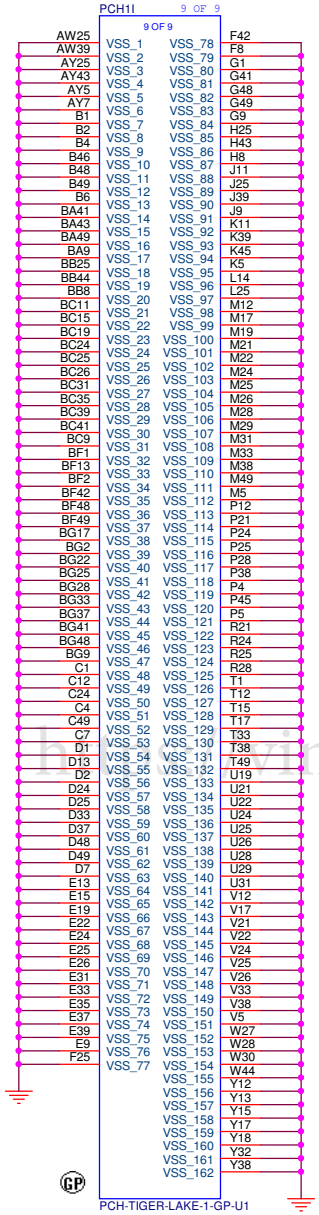
Title	PCH (POWER&Cap)	
Size A3	Document Number Cyborg_TGL-H RTX	Rev X01
Date: Friday, November 20, 2020	Sheet 22 of 106	



ZZ.00PCH.021



ZZ.00PCH.021

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TGL-H

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size: A3 | Document Number: Cyborg_TGL-H RTX | Rev: X01

Date: Friday, November 20, 2020 | Sheet 23 of 106

Main Func = KBC

#	MODEL_ID(GPIO202)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	GTX 15" DIS	100K	10K	3
2	GTX 16" DIS	100K	17.8K	2.801
3	RTX 16" DIS	100K	27K	2.598
4		100K	37.4K	2.402
5	GTX 16" UMA	100K	49.9K	2.201
6	GTX 15" UMA	100K	64.9K	2.001
7		100K	82.5K	1.808
8		100K	107K	1.594
9		100K	154K	1.299
10		100K	200K	1.1

17.8K_PN:64.17825.6DL

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	**10.0K**	3
2	X01	100.0K	**17.8K**	2.801
3	X02	100.0K	**27.0K**	2.598
4	X03(reserve)	100.0K	**37.4K**	2.402
5	A00	100.0K	**49.9K**	2.201
6	A01	100.0K	**64.9K**	2.001
7	A02	100.0K	**82.5K**	1.808
8	A03	100.0K	**107K**	1.594
9	Reserve	100.0K	**154K**	1.299
10	Reserve	100.0K	**200K**	1.1
11	Reserve	100.0K	**TBD**	0.9
12	Reserve	100.0K	**TBD**	0.7
13	Reserve	100.0K	**TBD**	0.5
14	Reserve	100.0K	**TBD**	0.3

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TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO055/SHD_CS 0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for BootNote 2 0=Use the eSPI Flash Channel for Boot Note 1	VTR2

Note 1: If the eSPI Flash Channel is used for booting, i.e., eSPI Master Attached Flash Sharing (MAFS), the GPIO055/PWM2/SHD_CS0# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. In addition, the GPIO016/GPT-P_IN1/SHD_IO3/ICT3 pin must be used as DSW_PWROK.This pin will also be driven high by the boot ROM code to support Deep Sleep Well timing requirements

2: If the Shared SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

3: The comparator strap option is an optional feature that may be enabled in OTP to enable the Boot ROM to configure and lock the Comparator 0 pins. If the feature is enabled in OTP, and external pull-up/pull-down is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the CMP_STRAP is not supported and no external pull-up or pull-down required. Application firmware may enable the comparator if supported by the specific package.

2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/SHD_CS0# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/SHD_CS0# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS0# pin on the board if the Shared SPI flash interface is used so that the SPI CS0# is detected hich while RSMRST# is low.

R2521.R2524.R2518.R2526.R2520 R2523.R2517.R2525.R2519.R2522	
SPI ROM	DY
SHARE ROM	15 ohm 64.49R95.6DL

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KBC MEC1515	
Cyborg_TGL-H RTX	X01
Tuesday, November 26, 2019	

SSID = Flash.ROM

SPI FLASH ROM (32M byte) for PCH

R2521.R2524.R2518.R2526.R2520 R2523.R2517.R2525.R2519.R2522	
SPI ROM	33 ohm 64.33R05.6DL
SHARE ROM	15 ohm 63.15034.1DL

18,24 SPI_CS_ROM_N0
18,24,91 SPI_SO_CPU
11,18,24 SPI_WP_CPU
11,18,24 SPI_HOLD_CPU
18,24,91 SPI_CLK_CPU
11,18,24,91 SPI_SI_CPU
18,24 SPI_CS_ROM_N1
20 RTC_DET#_PCH
24 RTCRST_ON
24 VCCDSW_EN#
17,40,45 3V_5V_POK
53 3V_5V_DSW_OK

3D3V_S5_PCH
C2501 SC10U6D3V3MX-DL-GP
C2502 SCD1U16V2KX-3DLGP

R2501 4K7R2J-2-GP
SPI25
W25Q256JVEIQ-GP
32M
072.25256.0N01

SKT2502
SKT-SPI8P-13-GP
062.10029.0091

R2502 4K7R2J-2-GP
SPI251
MX25L12872FM2I-10G-GP
072.25128.0D61

SKT2501
SKT-SPI8P-13-GP
062.10029.0091

Main Func = RTC

RTC GEN9

3D3V_S5
R2509 100KR2J-1-GP
VCCDSW_EN#
C2505 SC1U10V2KX-1GP
3V_5V_POK
D2502 BAT54A-11-GP
75.BAT54.07D
2ND = 75.00054.Q7D
R2510 10KR2J-3-GP
3V_5V_DSW_OK
U2502 RT9742CGJ5-GP
C2506 SC10U6D3V3MX-DL-GP
074.09742.0A9F
2nd = 074.51712.009F

3D3V_RTC_AUX
Q2501 PJA3413-1-GP
084.03413.0031
2nd = 084.02301.0031
RTC_AUX_S5
R2514 4K7R2J-2-GP
RTC_3P3_EN_D
Q2502 2N7002K-2-GP-U
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.131
4th = 84.2N702.W31
RTCRST_ON
R2512 1MR2J-1-GP
R2513 100KR2J-1-GP
RTC_3P3_EN_G
C2504 SCD022U16V2KX-3DLGP

3D3V_AUX_S5
R2505 0R2J-2-GP
3D3V_RTC_SYS
R2503 47KR2F-GP
D2501 BAT54C-12-GP
75.00054.A7D
3D3V_RTC_AUX
C2503 SCD47U25V2KX-1-GP
BATT_RTC
3D3V_S5_PCH
R2541 10KR2J-3-GP
R2504 10MR2J-L-GP
Q2505 2N7002K-2-GP-U
84.2N702.J31
2ND = 84.2N702.031
RTC_DET#_PCH

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TGL-H

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Title: Flash/RTC
Size: A2
Document Number: Cyborg_TGL-H RTX
Rev: X01
Date: Friday, November 20, 2020
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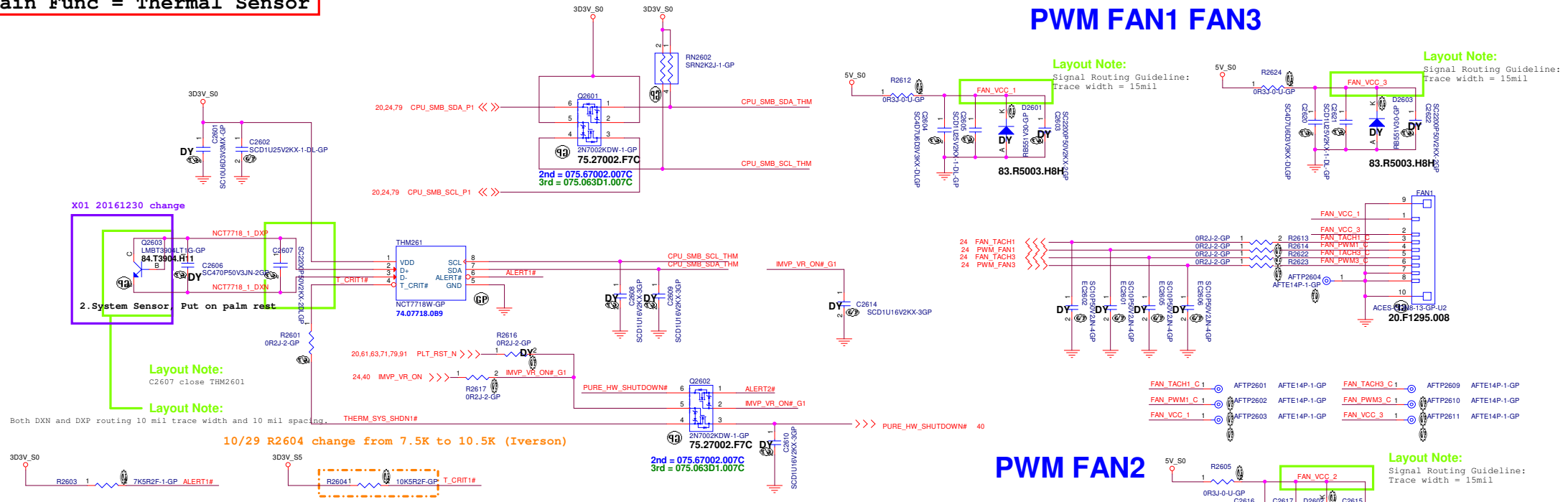
Main Func = Thermal Sensor



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

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Title: INT IO (Thermal/Fan)

Size: Custom | Document Number: Cyborg_TGL-H RTX | Rev: X01

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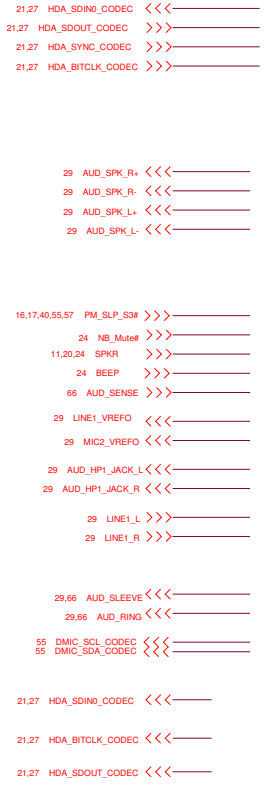
Main Func = Audio



Audio Codec Chip ALC3204

Analog
Digital

1.8V power rail should be supplied by linear regulator, not switching regulator.if switch regulator is unavailable, please make sure that switch frequency operates at out-band(over 20KHz)

>2A moat

ALC3204
QFN40 (5X5)
071.03204.0003

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

DVDD must >= DVDD_IO

Layout Note:
Place close to Pin 20

Layout Note:
Tied at point only under Codec or near the Codec

Analog
Digital
moat

place close to pin8

For RTC Gen9 reset circuit change power rail. 20170921

Open drain output. pull up to DVDD or max. 5V

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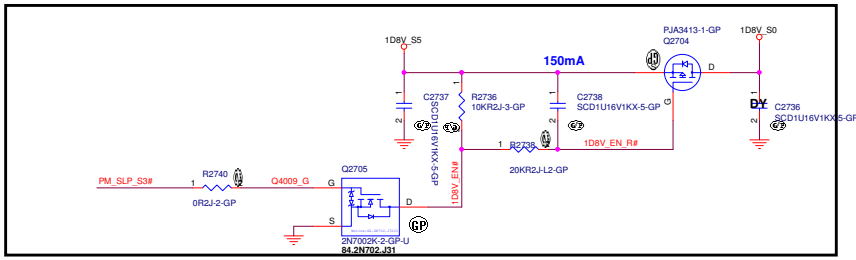
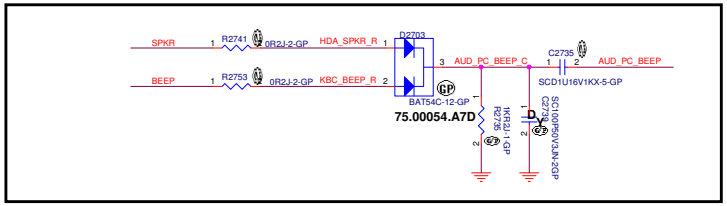
150mA





TGL-H

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Title: Audio (Codec ALC3204)

Size: Custom | Document Number: Cyborg_TGL-H RTX | Rev: X01

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TGL-H

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Title: *Audio (RSVD)*

Size: A3 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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Main Func = Audio

27 AUD_SPK_L+
27 AUD_SPK_L-
27 AUD_SPK_R+
27 AUD_SPK_R-

21 SPK_ID
27,29 LINE1_L
27,29 LINE1_R

From Codec

27 MIC2_VREFO

27 AUD_HP1_JACK_L
27,29 LINE1_L
27,29 LINE1_R
27 AUD_HP1_JACK_R

27 LINE1_VREFO

To IO Board

27,66 AUD_RING
66 AUD_HP1_JACK_L1
66 AUD_HP1_JACK_R1
27,66 AUD_SLEEVE

Speaker

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

AUD_SPK_R+ — R2904 1 — 0R3J-0-U-GP — AUD_SPK_R+_C
AUD_SPK_R- — R2903 1 — 0R3J-0-U-GP — AUD_SPK_R-_C
AUD_SPK_L- — R2901 1 — 0R3J-0-U-GP — AUD_SPK_L-_C
AUD_SPK_L+ — R2902 1 — 0R3J-0-U-GP — AUD_SPK_L+_C
SPK_ID

AUD_SPK_L-_C 1 — AFTP2901 AFTE14P-1-GP
AUD_SPK_L+_C 1 — AFTP2902 AFTE14P-1-GP
AUD_SPK_R-_C 1 — AFTP2903 AFTE14P-1-GP
AUD_SPK_R+_C 1 — AFTP2904 AFTE14P-1-GP

AZ5725-01FDR7G-GP DY D2903
AZ5725-01FDR7G-GP DY D2904
AZ5725-01FDR7G-GP DY D2905
AZ5725-01FDR7G-GP DY D2906

SC1KP50V2KX-1DLGP EC2901
SC1KP50V2KX-1DLGP EC2902
SC1KP50V2KX-1DLGP EC2903
SC1KP50V2KX-1DLGP EC2904

SPK1
7
1
2
3
4
5
6
8
ACES-CON6-20-GP-U
20.F1639.006

12/17 Clark move close to connector

MIC2_VREFO — RN2902 — SRN2K2J-1-GP

AUD_HP1_JACK_L — LINE1_L C2911 1 — SC10U6D3V3MX-DL-GP — LINE1-L_C — R2922 1 — 1KR2J-1-GP
AUD_HP1_JACK_R — LINE1_R C2910 1 — SC10U6D3V3MX-DL-GP — LINE1-L_R — R2921 1 — 1KR2J-1-GP

R2911 1 — 10R2F-L-GP — AUD_RING / AUD_HP1_JACK_L1
R2919 1 — 10R2F-L-GP — AUD_HP1_JACK_R1 / AUD_SLEEVE

D2902
LINE1_VREFO 3
1 — LINE1_VREFO_D1 — R2917 4K7R2J-2-GP
2 — LINE1_VREFO_D2 — R2918 4K7R2J-2-GP
BAT54A-11-GP
75.BAT54.07D

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Title: Audio (HP/SPK/MIC Jack)

Size	Document Number	Rev
Custom	Cyborg_TGL-H RTX	X01

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Title: *Audio (RSVD)*

Size: A3 | Document Number: Cyborg_TGL-H RTX | Rev: X01

Date: Friday, November 20, 2020 | Sheet 30 of 106

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Title: *LAN (RSVD)*

Size	Document Number	Rev
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Title: *LAN (RSVD)*

Size	Document Number	Rev
A3	Cyborg_TGL-H RTX	X01

Date: Friday, November 20, 2020 Sheet 32 of 106

SSID = Card Reader

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size: A3 | Document Number: Cyborg_TGL-H RTX | Rev: X01

Date: Friday, November 20, 2020 | Sheet 33 of 106

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TGL-H

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size: A3 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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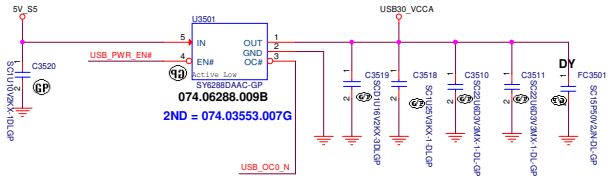
18 USB2_USB20_P
18 USB2_USB20_N

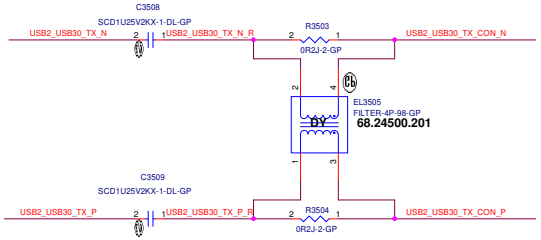
18 USB2_USB30_RX_N
18 USB2_USB30_RX_P

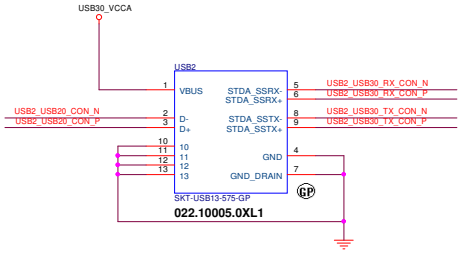
18 USB2_USB30_TX_N
18 USB2_USB30_TX_P

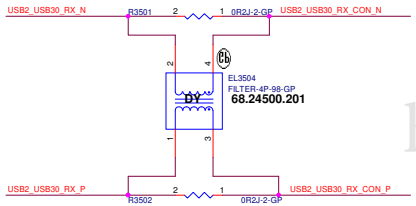
21 USB_OC0_N

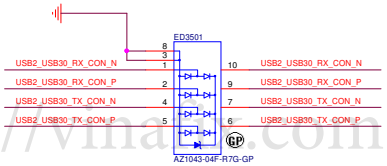
24,66 USB_PWR_EN#

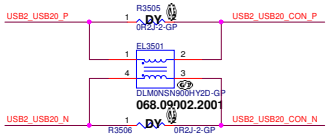


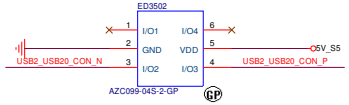












USB 3.0 Connector Pin definition

1	POWER
2	USB 2.0 D–
3	USB 2.0 D+
4	GND
5	StdA_SSRX– SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX– SuperSpeed TX
9	StdA_SSTX+

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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (REAR IO/ USB3.0 Conn)

Size: A2 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB (RSVD)*

Size	Document Number	Rev
A3	Cyborg_TGL-H RTX	X01

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Wistron Corporation
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Title: *USB (RSVD)*

Size	Document Number	Rev
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SSID = USB3.0 Redrivere

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Title: *USB (RSVD)*

Size	Document Number	Rev
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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Sequence(RSVD)*

Size: A3 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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Power Sequence

5V_S0

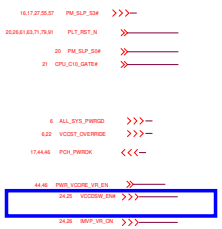
5V_S0 Consumption
Peak current 5A

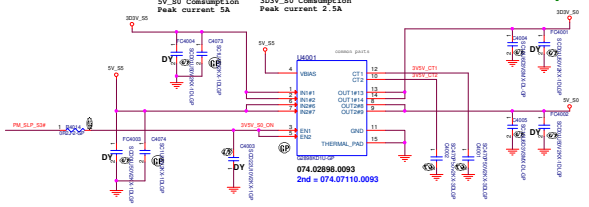
3D3V_S0

3D3V_S0 Consumption
Peak current 2.5A

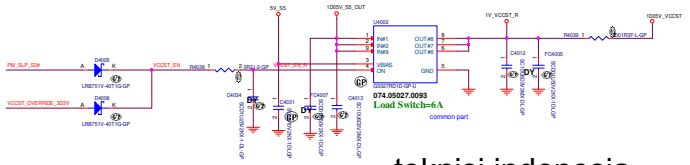
ROSA Run Power

6A Continuous Switch Current per channel





1V_VCCST



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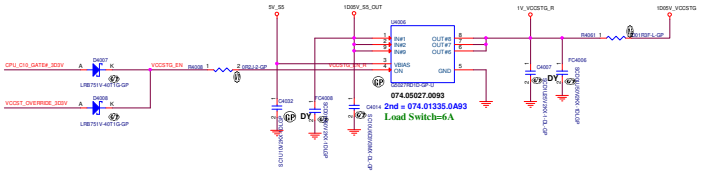
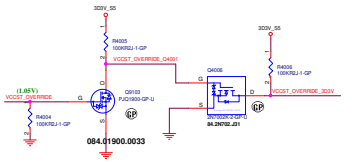
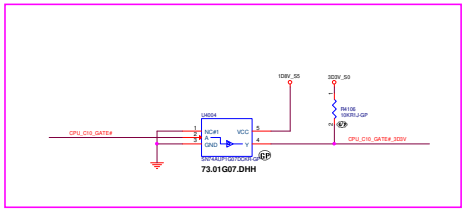
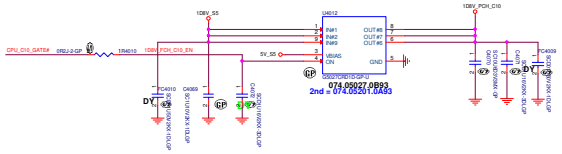
1V_VCCSTG

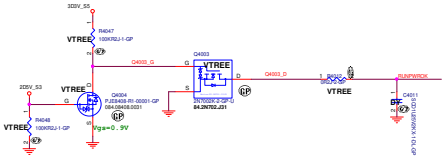








V_TREE



PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	0.3	0.64	0.9	V

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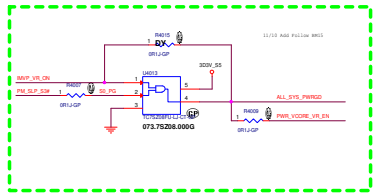
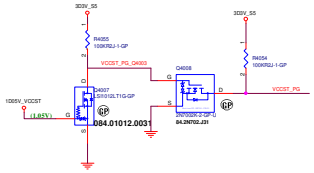
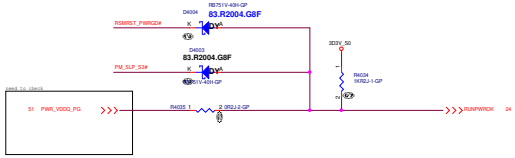
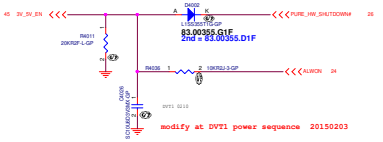
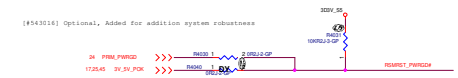
Power Sequence / Pull High PWRGD











Wistron Corporation	21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Sequence (Power on)
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Main Func = Power & Sequence

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TGL-H

Wistron Corporation
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Title: *Sequence (DS3/S0ix)*

Size	Document Number	Rev
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TGL-H

Wistron Corporation
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Title: *INT IO (Current meter)*

Size	Document Number	Rev
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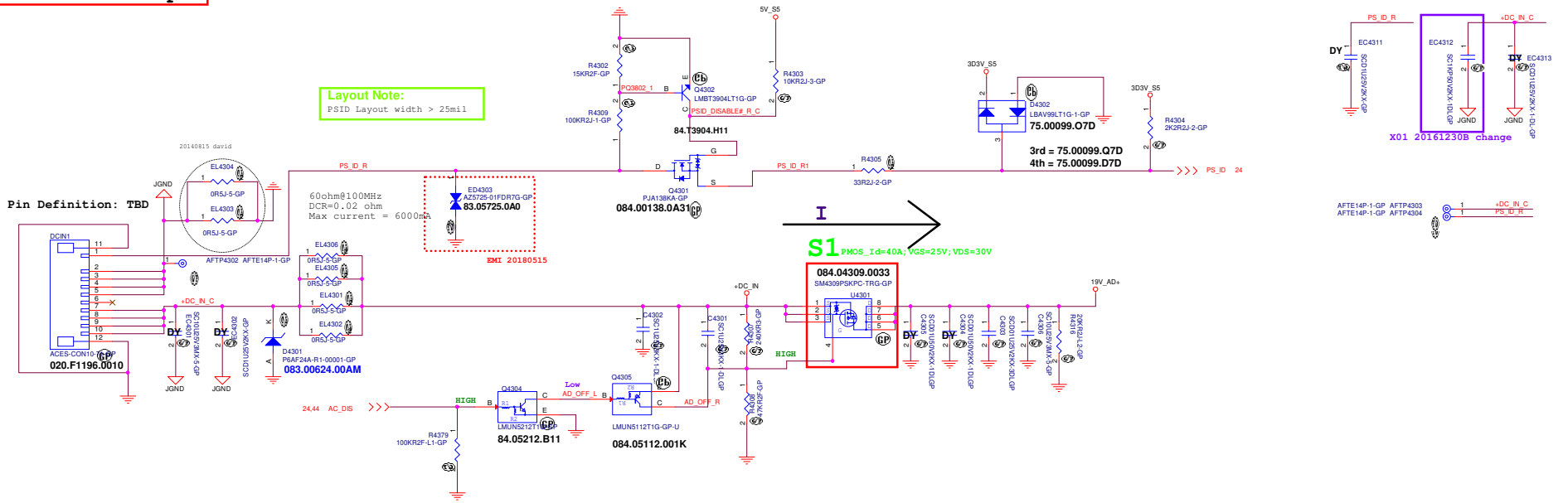
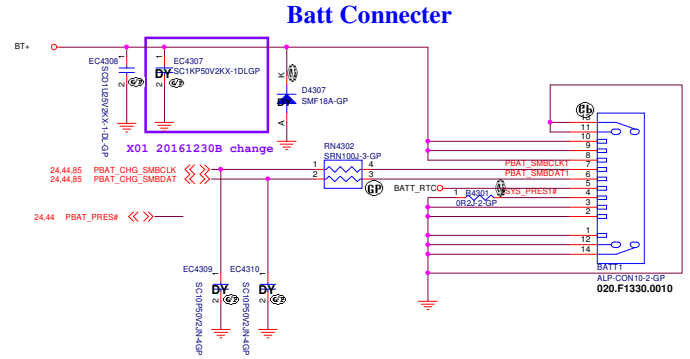
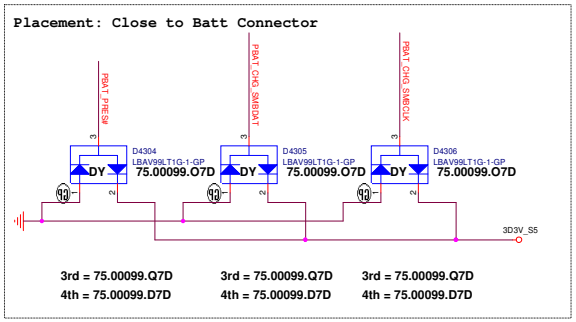
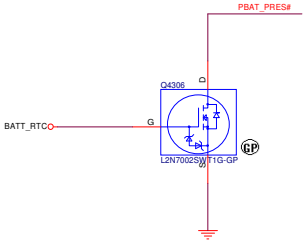
Main Func = ADT Input

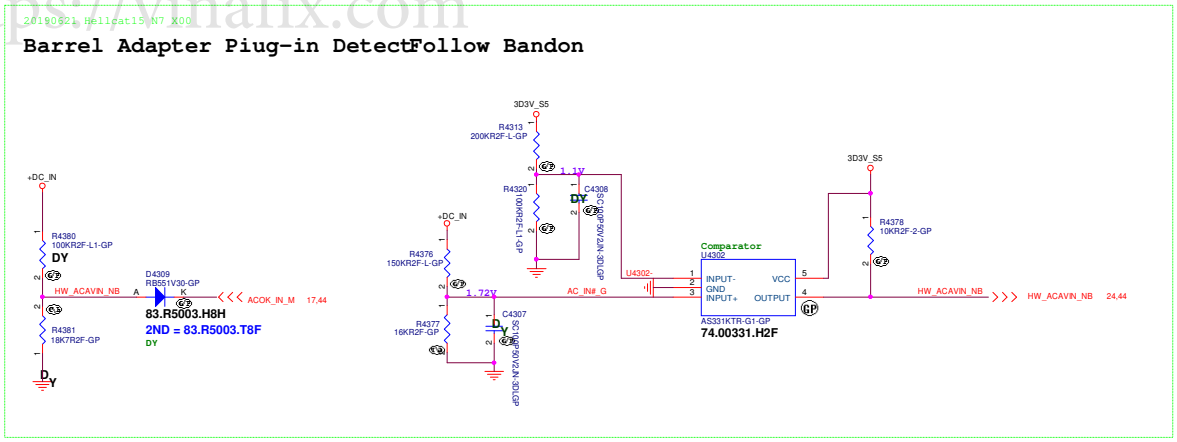


Main Func = M-BAT Input









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Title: INT IO (ATX/ DC/ BATT Conn)

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ISL9538C For Charger

Main Func = Charger

OFFPAGE

EE needs check it!!

I2C form EC

To EC

ISL9538 AMON/BMON to EC

From NXP ACK

OVP

E3

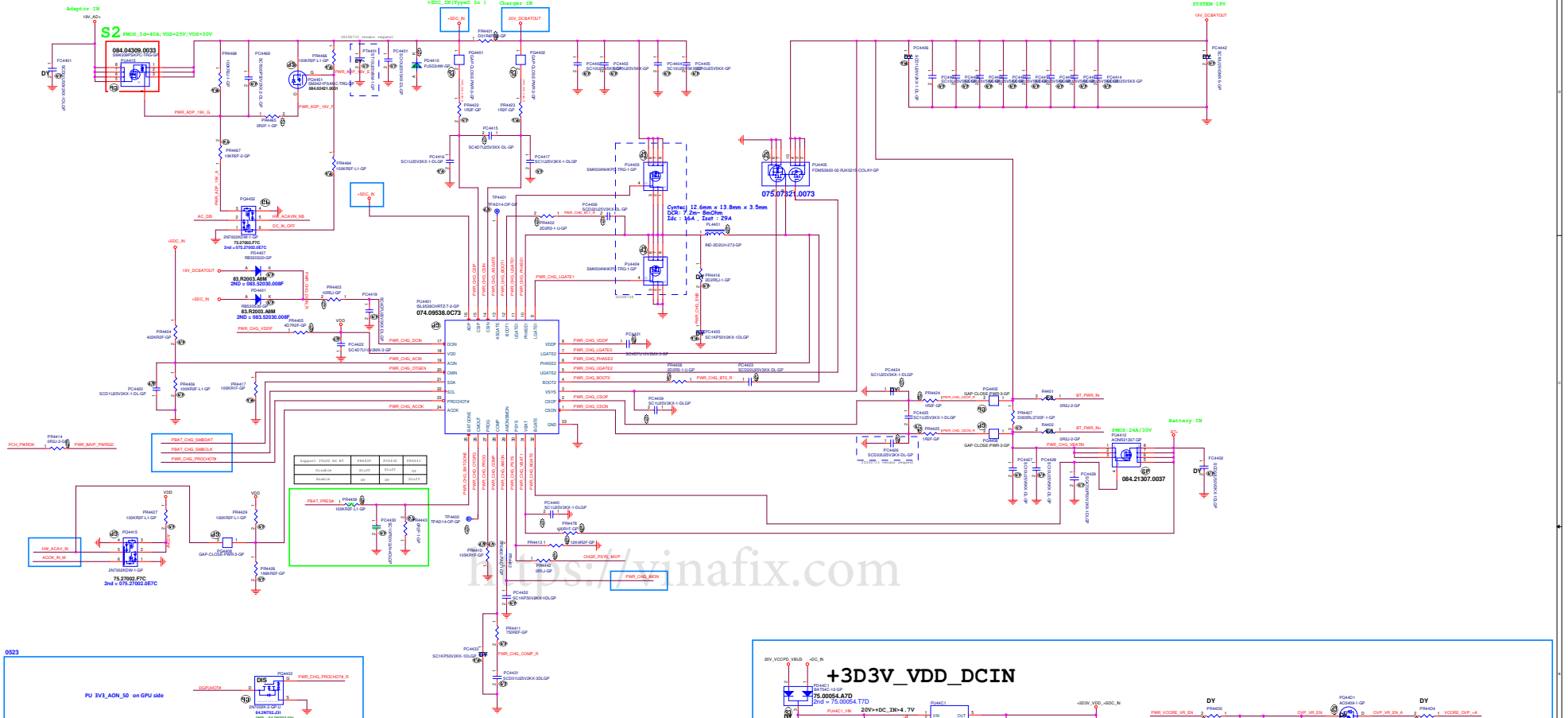

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TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLIm&L Reg(A)
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

INTEL CONFIDENTIAL NEVO

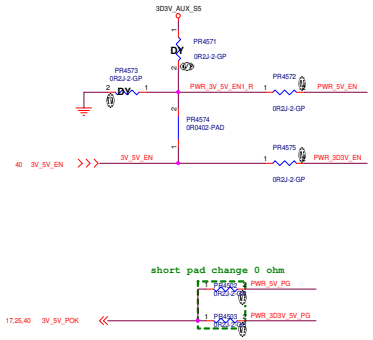
Wistron Corporation

Power (Charger_ISL9538)

Cyborg_TGL-H RTX

SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal



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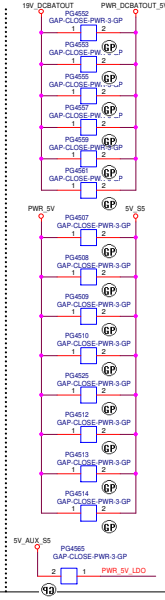

SY8288C For 5V

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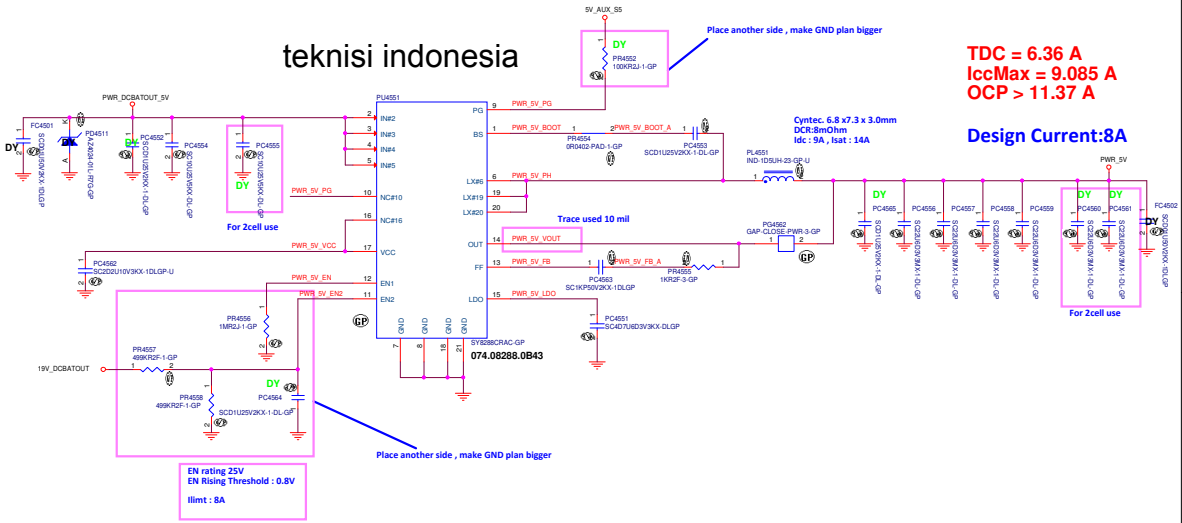
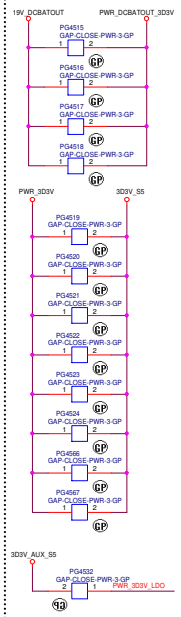


SSID = PWR.Plane.Regulator_3D3V

OFFPAGE-Signal

OFFPAGE-GAP



TPS51393 For 3D3V

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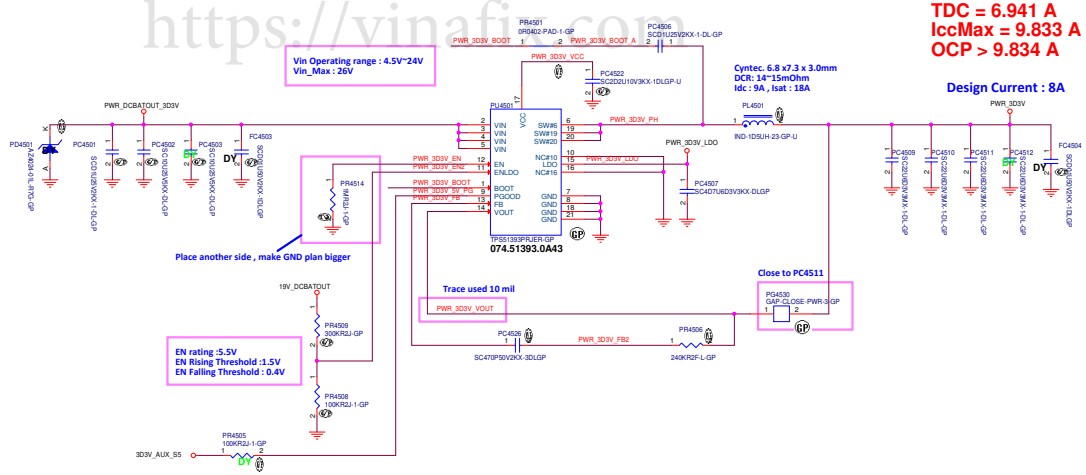

TGL-H

DELL Wistron Corporation
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Title: POWER (SY8288_5V/TPS51393_3D3V)

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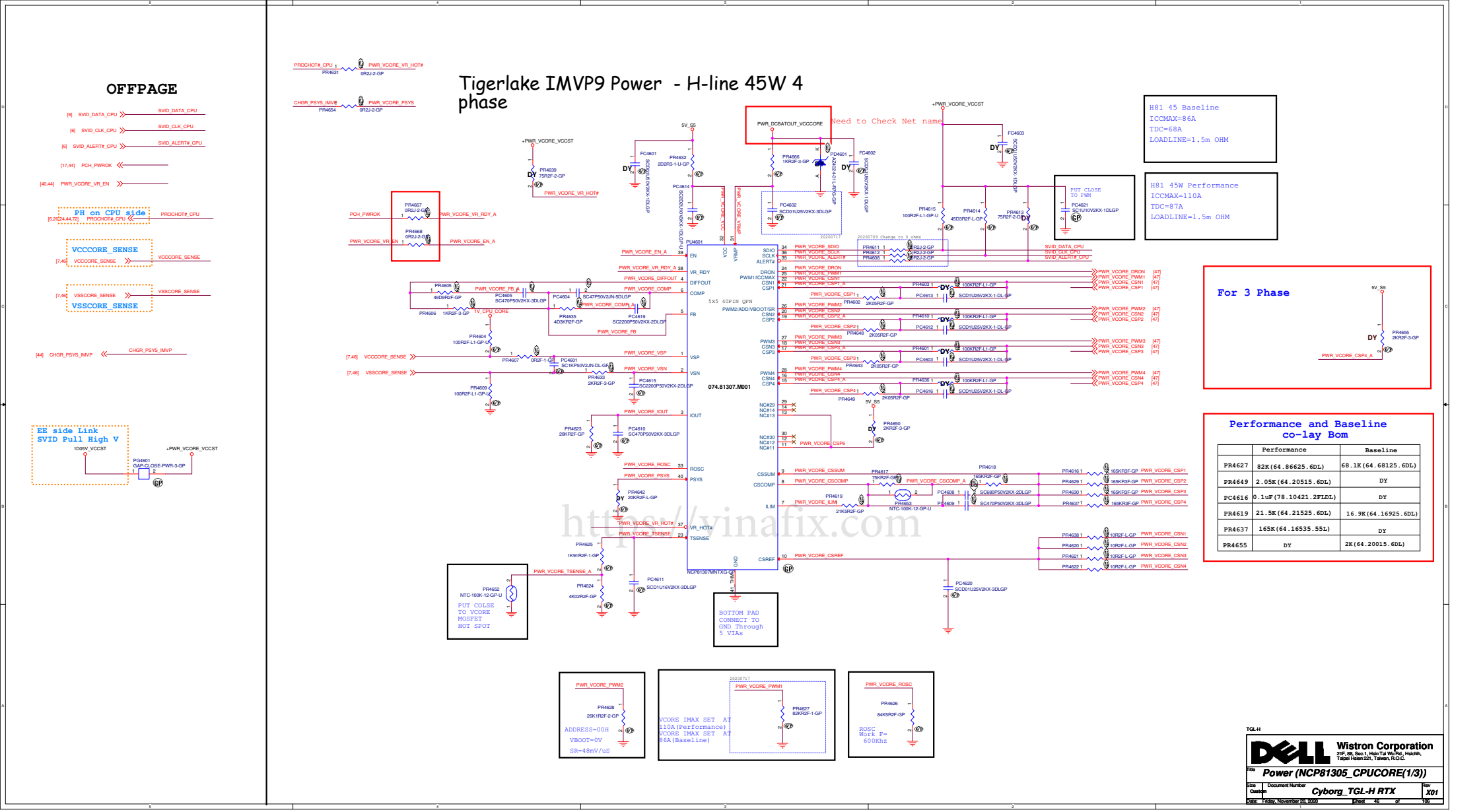
OFFPAGE
[6] SVID_DATA_CPU
SVID_DATA_CPU
[6] SVID_CLK_CPU
SVID_CLK_CPU
[6] SVID_ALERT#_CPU
SVID_ALERT#_CPU
[17,44] PCH_PWROK
[40,44] PWR_VCORE_VR_EN
PH on CPU side
[6,20,24,44,72] PROCHOT#_CPU
PROCHOT#_CPU
VCCCORE_SENSE
[7,46] VCCCORE_SENSE
VCCCORE_SENSE
[7,46] VSSCORE_SENSE
VSSCORE_SENSE
VSSCORE_SENSE
[44] CHGR_PSYS_IMVP
CHGR_PSYS_IMVP
EE side Link
SVID Pull High V
1D05V_VCCST
+PWR_VCORE_VCCST
PG4601
GAP-CLOSE-PWR-3-GP
PROCHOT#_CPU
PR4631
0R2J-2-GP
PWR_VCORE_VR_HOT#
CHGR_PSYS_IMVP
PR4654
0R2J-2-GP
PWR_VCORE_PSYS
Tigerlake IMVP9 Power - H-line 45W 4 phase
H81 45 Baseline
ICCMAX=86A
TDC=68A
LOADLINE=1.5m OHM
H81 45W Performance
ICCMAX=110A
TDC=87A
LOADLINE=1.5m OHM
PWR_DCBATOUT_VCCCORE
Need to Check Net name
+PWR_VCORE_VCCST
5V_S5
PU4601
074.81307.M001
5X5 40PIN QFN
NCP81307MNTXG-GP
PWR_VCORE_VR_RDY_A
PWR_VCORE_EN_A
PWR_VCORE_DIFFOUT
PWR_VCORE_COMP
PWR_VCORE_FB
PWR_VCORE_VSP
PWR_VCORE_VSN
PWR_VCORE_IOUT
PWR_VCORE_ROSC
PWR_VCORE_PSYS
PWR_VCORE_VR_HOT#
PWR_VCORE_TSENSE
PWR_VCORE_CSREF
PWR_VCORE_CSSUM
PWR_VCORE_CSCOMP
PWR_VCORE_ILIM
PWR_VCORE_SDIO
PWR_VCORE_SCLK
PWR_VCORE_ALERT#
PWR_VCORE_DRON
PWR_VCORE_PWM1
PWR_VCORE_CSN1
PWR_VCORE_CSP1
PWR_VCORE_PWM2
PWR_VCORE_CSN2
PWR_VCORE_CSP2
PWR_VCORE_PWM3
PWR_VCORE_CSN3
PWR_VCORE_CSP3
PWR_VCORE_PWM4
PWR_VCORE_CSN4
PWR_VCORE_CSP4
PCH_PWROK
PWR_VCORE_VR_RDY_A
PWR_VCORE_VR_EN
PWR_VCORE_EN_A
PUT CLOSE TO PWM
PUT COLSE TO VCORE MOSFET HOT SPOT
BOTTOM PAD CONNECT TO GND Through 5 VIAs
VCORE IMAX SET AT 110A(Performance)
VCORE IMAX SET AT 86A(Baseline)
ADDRESS=00H
VBOOT=0V
SR=48mV/uS
ROSC Work F= 600Khz
For 3 Phase
Performance and Baseline co-lay Bom
Performance
Baseline
PR4627 82K(64.86625.6DL) 68.1K(64.68125.6DL)
PR4649 2.05K(64.20515.6DL) DY
PC4616 0.1uF(78.10421.2FLDL) DY
PR4619 21.5K(64.21525.6DL) 16.9K(64.16925.6DL)
PR4637 165K(64.16535.55L) DY
PR4655 DY 2K(64.20015.6DL)
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TGL-H
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
Power (NCP81305_CPUCORE(1/3))
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46 PWR_VCORE_DRON — PWR_VCORE_DRON

46 PWR_VCORE_PWM1 — PWR_VCORE_PWM1
46 PWR_VCORE_PWM2 — PWR_VCORE_PWM2
46 PWR_VCORE_PWM3 — PWR_VCORE_PWM3
46 PWR_VCORE_PWM4 — PWR_VCORE_PWM4

46 PWR_VCORE_CSP1 — PWR_VCORE_CSP1
46 PWR_VCORE_CSN1 — PWR_VCORE_CSN1
46 PWR_VCORE_CSP2 — PWR_VCORE_CSP2
46 PWR_VCORE_CSN2 — PWR_VCORE_CSN2
46 PWR_VCORE_CSP3 — PWR_VCORE_CSP3
46 PWR_VCORE_CSN3 — PWR_VCORE_CSN3
46 PWR_VCORE_CSP4 — PWR_VCORE_CSP4
46 PWR_VCORE_CSN4 — PWR_VCORE_CSN4

19V_DCBATOUT — PWR_DCBATOUT_VCCCORE — 19V_DCBATOUT

PG4770 … PG4779 — GAP-CLOSE-PWR-3-GP

PG4780 … PG4783 — GAP-CLOSE-PWR-3-GP

19V_DCBATOUT

PC4767 330UF-0EL025V06M-1-GP — PC4768 330UF-0EL025V06M-1-GP

077.C1071.0071
2nd = 077.C1071.0101

077.C2261.0041

Acoustic

33uF/25V,
ESR=42mohm,
Ripple_Current=3200mA

Phase1

Max Current = 3.50(A)

PWR_DCBATOUT_VCCCORE

PC4701 … PC4710 — 47UF-0EL025V06M-1-GP

PC4711 … PC4720 — 47UF-0EL025V06M-1-GP

PR4703 20.0KR1-GP — PWR_CORE_BOOT_PH1

PR4704 — PWR_CORE_BOOT_A_PH1

PC4703 SCD33U16V3KX-4-GP — PWR_CORE_PHASED_PH1

PR4701 2.55R1-GP — PWR_CORE_VCCA

PC4701 — PC4702 SCY10V100KX-1GP

PU4701 — 074.30204.0AE3

PR4705 — PWR_CORE_DRVH_PH1

PR4706 — PWR_CORE_DRVL_PH1

PR4707 — PWR_CORE_THWN_PH1

PR4708 — PWR_CORE_SWNP_PH1

PR4709 — PWR_CORE_SWNN_PH1

PR4710 — PWR_CORE_CSNP_PH1

PR4711 — PWR_CORE_CSNN_PH1

PR4712 — PWR_CORE_CSCOMP_PH1

PR4713 — PWR_CORE_CSREF_PH1

PR4714 — PWR_CORE_ISUM_PH1

PR4715 — PWR_CORE_ISEN_PH1

PR4716 — PWR_CORE_VSEN_PH1

PR4717 — PWR_CORE_RTN_PH1

PR4718 — PWR_CORE_FB_PH1

PR4719 — PWR_CORE_COMP_PH1

PR4720 — PWR_CORE_PH1

PR4721 — PWR_CORE_VCCB

PR4722 — PWR_CORE_BOOT_PH2

PR4723 — PWR_CORE_BOOT_A_PH2

PR4724 — PWR_CORE_PHASED_PH2

PC4721 — PC4722 SCY10V100KX-1GP

PU4702 — 074.30204.0AE3

PR4725 — PWR_CORE_DRVH_PH2

PR4726 — PWR_CORE_DRVL_PH2

PR4727 — PWR_CORE_THWN_PH2

PR4728 — PWR_CORE_SWNP_PH2

PR4729 — PWR_CORE_SWNN_PH2

PR4730 — PWR_CORE_CSNP_PH2

PR4731 — PWR_CORE_CSNN_PH2

PR4732 — PWR_CORE_CSCOMP_PH2

PR4733 — PWR_CORE_CSREF_PH2

PR4734 — PWR_CORE_ISUM_PH2

PR4735 — PWR_CORE_ISEN_PH2

PR4736 — PWR_CORE_VSEN_PH2

PR4737 — PWR_CORE_RTN_PH2

PR4738 — PWR_CORE_FB_PH2

PR4739 — PWR_CORE_COMP_PH2

PR4740 — PWR_CORE_PH2

PR4741 — PWR_CORE_VCCC

PR4742 20.0KR1-GP — PWR_CORE_BOOT_PH3

PR4743 — PWR_CORE_BOOT_A_PH3

PR4744 SCD33U16V3KX-4-GP — PWR_CORE_PHASED_PH3

PC4741 — PC4742 SCY10V100KX-1GP

PU4703 — 074.30204.0AE3

PR4745 — PWR_CORE_DRVH_PH3

PR4746 — PWR_CORE_DRVL_PH3

PR4747 — PWR_CORE_THWN_PH3

PR4748 — PWR_CORE_SWNP_PH3

PR4749 — PWR_CORE_SWNN_PH3

PR4750 — PWR_CORE_CSNP_PH3

PR4751 — PWR_CORE_CSNN_PH3

PR4752 — PWR_CORE_CSCOMP_PH3

PR4753 — PWR_CORE_CSREF_PH3

PR4754 — PWR_CORE_ISUM_PH3

PR4755 — PWR_CORE_ISEN_PH3

PR4756 — PWR_CORE_VSEN_PH3

PR4757 — PWR_CORE_RTN_PH3

PR4758 — PWR_CORE_FB_PH3

PR4759 — PWR_CORE_COMP_PH3

PR4760 — PWR_CORE_PH3

PR4761 — PWR_CORE_VCCD

PR4762 20.0KR1-GP — PWR_CORE_BOOT_PH4

PR4763 — PWR_CORE_BOOT_A_PH4

PR4764 SCD33U16V3KX-4-GP — PWR_CORE_PHASED_PH4

PC4761 — PC4762 SCY10V100KX-1GP

PU4704 — 074.30204.0AE3

PR4765 — PWR_CORE_DRVH_PH4

PR4766 — PWR_CORE_DRVL_PH4

PR4767 — PWR_CORE_THWN_PH4

PR4768 — PWR_CORE_SWNP_PH4

PR4769 — PWR_CORE_SWNN_PH4

PR4770 — PWR_CORE_CSNP_PH4

PR4771 — PWR_CORE_CSNN_PH4

PR4772 — PWR_CORE_CSCOMP_PH4

PR4773 — PWR_CORE_CSREF_PH4

PR4774 — PWR_CORE_ISUM_PH4

PR4775 — PWR_CORE_ISEN_PH4

PR4776 — PWR_CORE_VSEN_PH4

PR4777 — PWR_CORE_RTN_PH4

PR4778 — PWR_CORE_FB_PH4

PR4779 — PWR_CORE_COMP_PH4

PR4780 — PWR_CORE_PH4

PL4701 — PWR_CORE_PH1

PL4702 — PWR_CORE_PH2

PL4703 — PWR_CORE_PH3

PL4704 — PWR_CORE_PH4

PG4701 GAP-CLOSE-PWR-6-GP — PWR_VCORE_CSN1

PG4702 GAP-CLOSE-PWR-6-GP — PWR_VCORE_CSP1

PG4703 GAP-CLOSE-PWR-6-GP — PWR_VCORE_CSN2

PG4704 GAP-CLOSE-PWR-6-GP — PWR_VCORE_CSP2

PG4705 GAP-CLOSE-PWR-6-GP — PWR_VCORE_CSN3

PG4706 GAP-CLOSE-PWR-6-GP — PWR_VCORE_CSP3

PG4707 GAP-CLOSE-PWR-6-GP — PWR_VCORE_CSN4

PG4708 GAP-CLOSE-PWR-6-GP — PWR_VCORE_CSP4

1V_CPU_CORE

MLCCs must be placed symmetrically on Top and Bottom.

Phase2

Max Current = 3.50(A)

PWR_DCBATOUT_VCCCORE

MLCCs must be placed symmetrically on Top and Bottom.

Phase3

Max Current = 3.50(A)

PWR_DCBATOUT_VCCCORE

MLCCs must be placed symmetrically on Top and Bottom.

Phase4

Max Current = 3.50(A)

PWR_DCBATOUT_VCCCORE

MLCCs must be placed symmetrically on Top and Bottom.

This circuit is for Hexa core.
Please refer to the table in next page.

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TGL-H

DELL — Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (NCP302045_CPUCORE(2/3))

Size: C — Document Number: Cyborg_TGL-H RTX — Rev: 0.01

Date: Friday, November 06, 2020 — Sheet 37 of 46

https://vinafix.com

TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Power (RSVD)

Size	Document Number	Rev
A3	Cyborg_TGL-H RTX	X01

Date: Friday, November 20, 2020 Sheet 48 of 106

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TGL-H

DELL	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		
Size A3	Document Number **Cyborg_TGL-H RTX**	Rev **X01**
Date: Friday, November 20, 2020	Sheet 49 of 106	

RT6543 For VCCIN_AUX

OFFPAGE

OFFPAGE_GAP

PH on CPU side

VCCAUX_SENSE

VSSAUX_SENSE

OCP :37.8 A

HI = 800KHz
Flot = 600KHz
Low = 400KHz

EDC=42A
IDC=21A
OCP > 48A
FREQUENCY: ~400KHz
VIN RIPPLE CURRENT(EDC/TDC): ~9.263A/4.052A
INDUCTOR RIPPLE CURRENT(EDC/TDC):27.231A

Cyntec 6.8mm x7.3mmx 2.4mm
DCR: 2.2~2.8m Ohm
Idc : 25A , Isat : 50A

075.07321.0073

Close to choke

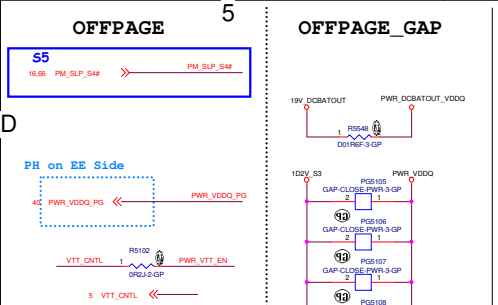
10MF / B=3370K

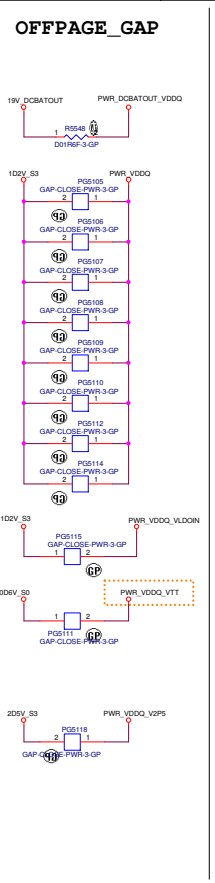
https://vinafix.com

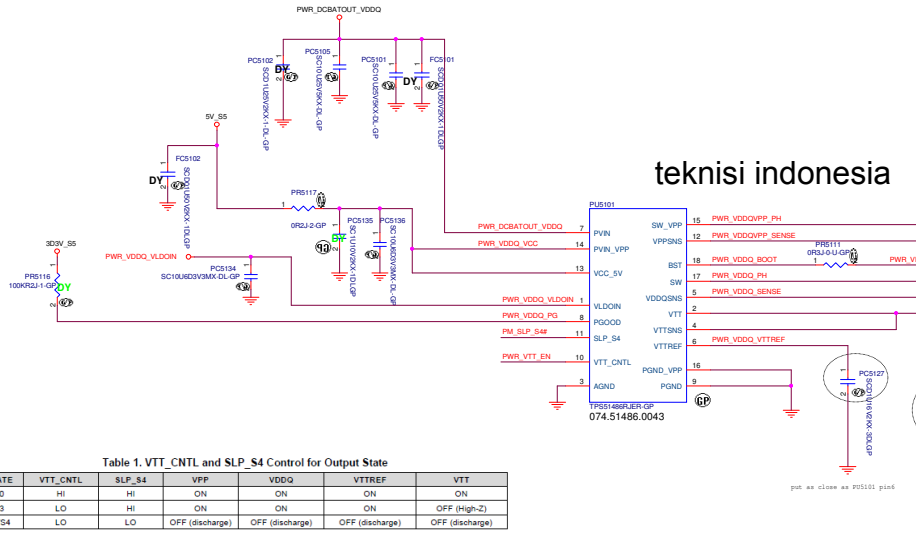
Wistron Corporation
RT6543 VCCAUX
Cyborg TGL-H RTX
X01

TPS51393 for VDDQ/VPP/VTT

Design current
VDDQ:8A
VTT:1A
2.5V:0.49A



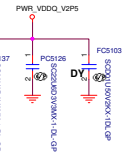




teknisi indonesia

murata. 2.5 x 2.0 x 1.2 mm
DCR:240mOhm
Idc : 1.3A , Isat : 1.5 A

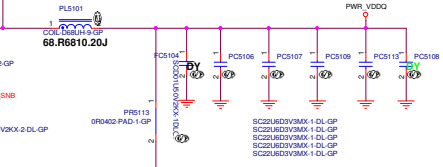
2D5V
Design Current : 0.49A



TDC :6.72 A
IccMax : 9.6 A

Cyntec. 6.6 x 7.3 x 3.0 mm
DCR: 4.8m~5.3 mOhm
Idc : 16 A , Isat : 17 A

VDDQ
Design Current : 8A



VTT
Design Current : 1A

Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

https://vinafix.com

TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (TPS51486_VDDQ/VTT/VPP)

Size	Document Number	Rev
Custom	Cyborg_TGL-H RTX	X01

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Main Func = VCCIN_AUX

RT6543 For PCH

OFFPAGE

VID

21,50 VCCAUX_VID0 — PR5211 0R2J-2-GP — PWR_VCCAUXPCH_VID0

21,50 VCCAUX_VID1 — PR5212 0R2J-2-GP — PWR_VCCAUXPCH_VID1

50,53 PWR_1D8V_PG — PR5223 0R2J-2-GP — PWR_VCCAUXPCH_EN

17,40,50 PWR_VCCAUX_PCH_PG — PR5220 0R2J-2-GP — PWR_VCCAUXPCH_PG

VCCIN_AUX SENSE

22 VCCAUX_PCH_SENSE — PR5214 0R2J-2-GP — PWR_VCCAUXPCH_FB_A

22 VSSAUX_PCH_SENSE — PR5215 0R2J-2-GP — PWR_VCCAUXPCH_RGND

19V_DCBATOUT — PR5221 — PR5222 — PWR_DCBATOUT_VCCAUXPCH

GAP-CLOSE-PWR-3-GP

GAP-CLOSE-PWR-3-GP

PWR_DCBATOUT_VCCAUXPCH

PC5204 SC10U25V5MX-5-GP

PC5205 SC10U25V5MX-5-GP

PC5210 SC10U25V5MX-5-GP

PC5211 SC10U25V5MX-5-GP

PD5201 AZ4624-01L-R7G-GP

PWR_VCCAUXPCH_BOOT

PC5207 SCD1U25V2KX-1-DL-GP

PWR_DCBATOUT_VCCAUXPCH

PR5224 2D2R2J-GP

PC5238 SCD1U25V2KX-1-DL-GP

PU5202 SM3380EHQGC-TRG-GP

TGL-H 42 45W
TDC=7A
ICCMAX=13A

Cyntec. 4.8mm x4.7mmx 3.0mm
DCR: 3.5~3.9m Ohm
Idc : 14A , Isat : 14.5A

3D3V_S5

5V_S5

PR5202 124KR2F-GP

PR5201 2D2R2J-GP

PR5204 10KR2J-3-GP

PR5203 10KR2J-3-GP

PC5206 SC1U10V2KX-1DLGP

PC5208 SC1U10V2KX-1DLGP

PU5201 RT6543AGQW-GP

074.06543.0073

CS_DIS, PVCC, VCC, PG, EN, VID1, VID0, FSWSEL, BOOT, VSYS, UG, PH, LG, PGND, ISENSEP, ISENSEN, VOUT, COMP, FB, RGND, AGND

PWR_VCCAUXPCH_CS_DIS, PWR_VCCAUXPCH_VCC, PWR_VCCAUXPCH_PG, PWR_VCCAUXPCH_EN, PWR_VCCAUXPCH_VID1, PWR_VCCAUXPCH_VID0, PWR_VCCAUXPCH_FSW, PWR_VCCAUXPCH_VSYS, PWR_VCCAUXPCH_UG, PWR_VCCAUXPCH_LX, PWR_VCCAUXPCH_LG, PWR_VCCAUXPCH_ISENP, PWR_VCCAUXPCH_ISENN, PWR_VCCAUXPCH_FB_A, PWR_VCCAUXPCH_COMP, PWR_VCCAUXPCH_FB, PWR_VCCAUXPCH_RGND

PL5201 COIL-D2UH-2-GP

1D8V_VCCINAUX_PCH

PG5201 GAP-CLOSE-PWR-3-GP

PG5202 GAP-CLOSE-PWR-3-GP

PWR_VCCAUXPCH_LXF

PR5217 17K8R2F-GP

PR5213 0R2J-2-GP

PWR_VCCAUXPCH_OUTF

PC5209 SCD1U25V2KX-1-DL-GP

PR5207 332R2F-1-GP

PR5218 634R2F-1-GP

PWR_VCCAUXPCH_RG

PR5219 NTC-10K-29-GP-U

B=3370K

PR5206 100R2F-L1-GP-U

PC5215 SC220U6D3VMX-1-DL-GP

PC5202 SC2200P50V2KX-2DLGP

PR5210 10KR2F-2-GP

PWR_VCCAUXPCH_COMP_R

PC5201 SC470P50V2KX-3DLGP

PR5208 1K6R2F-GP

PWR_VCCAUXPCH_FB_R

PC5203 SC22P50V2JN-4DLGP

PR5209 5K62R2F-GP

PR5205 100R2F-L1-GP-U

PWR_VCCAUXPCH_FB_A

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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT6543A_VCCAUXPCH

Size: A2 | Document Number | Rev: X01

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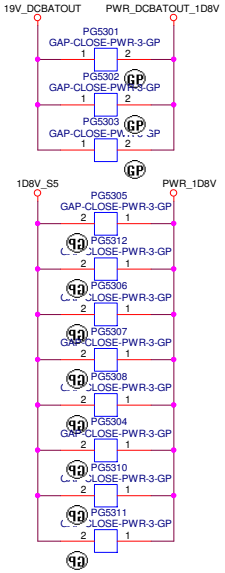
Main Func = 1D8V

OFFPAGE

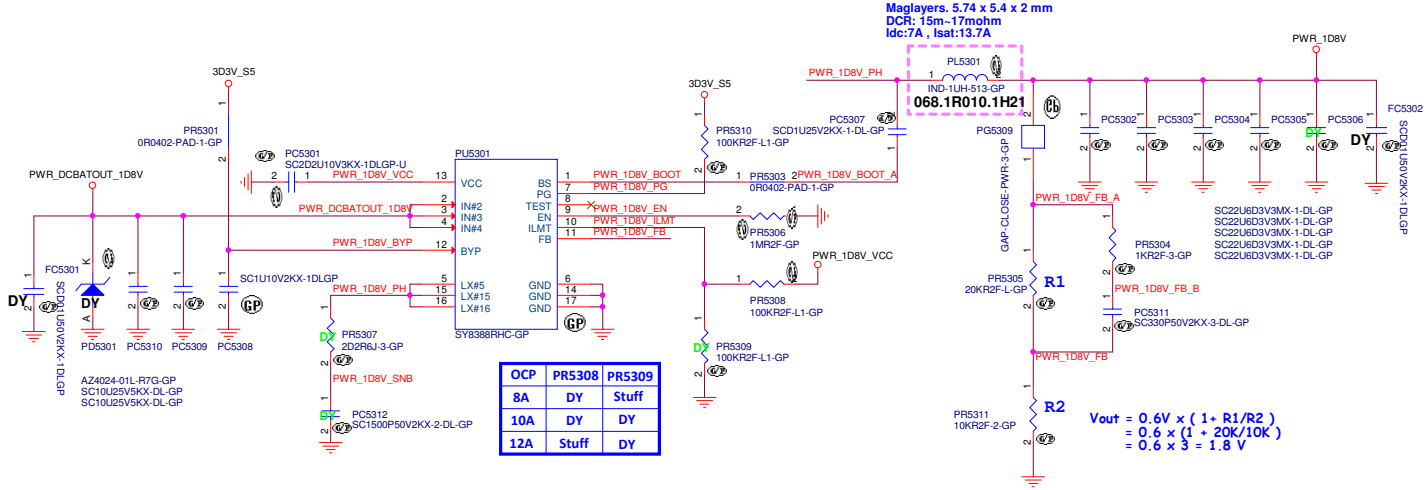
PH on EE Side

OFFPAGE_GAP

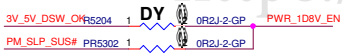


SY8388RHC for 1D8V

1D8V
TDC : 7.25 A
Iccmax : 9.05 A
OCP : 12A



OCP	PR5308	PR5309
8A	DY	Stuff
10A	DY	DY
12A	Stuff	DY



https://vinafix.com

TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (1D8V)

Size	Document Number	Rev
Custom	Cyborg_TGL-H RTX	X01

Date: Friday, November 20, 2020 Sheet 53 of 106

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no need VNN/V1P05V
Power for Volume design!!

https://vinafix.com

TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (VCCIO/VCC_PRIM /BYPSS/ 12V)

Size	Document Number	Rev
A3	Cyborg_TGL-H RTX	X01

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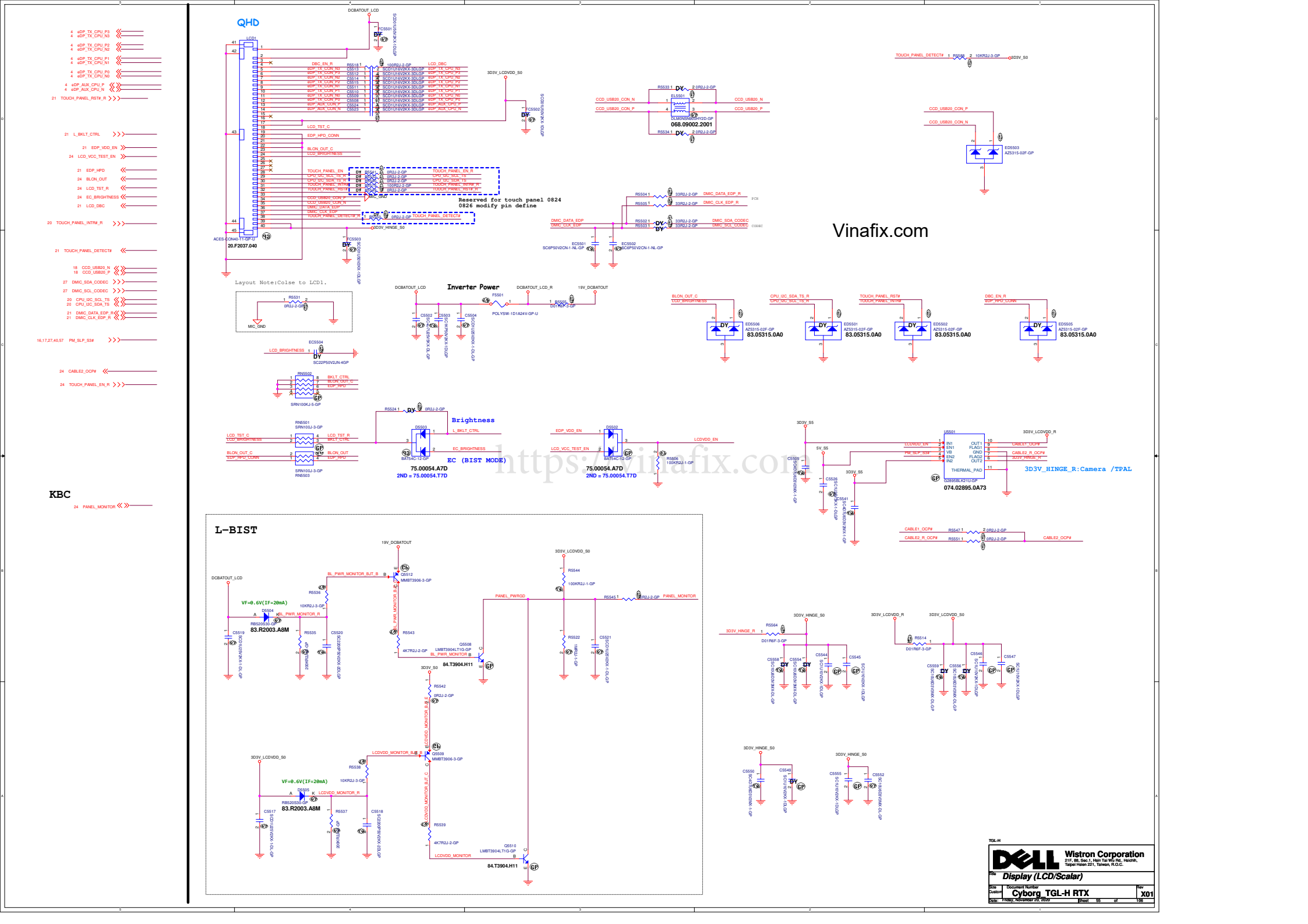

TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (LCD/Scalar)

Size	Document Number	Rev
Custom	Cyborg_TGL-H RTX	X01

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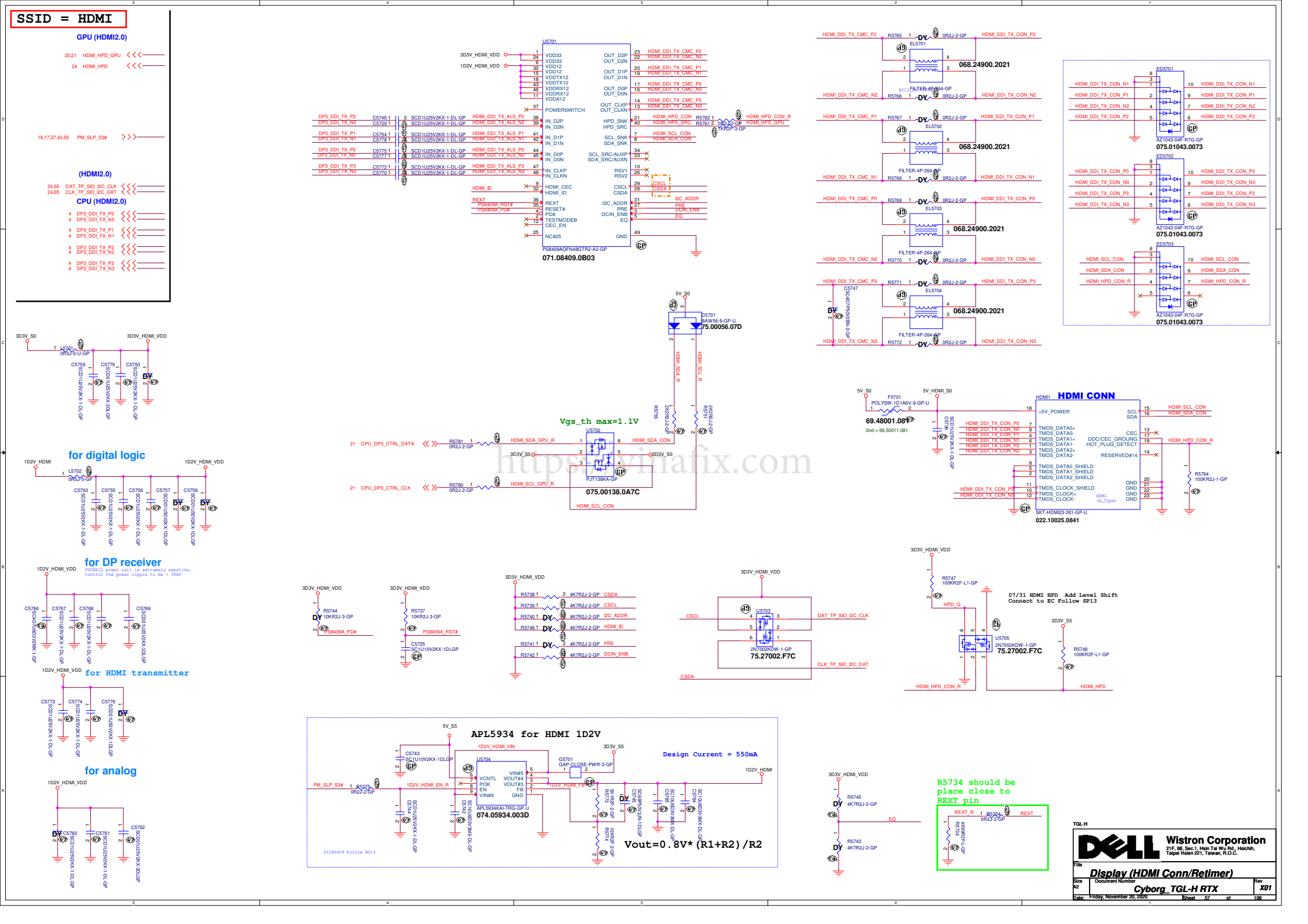
TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Display (CRT/IR Camera)*

Size	Document Number	Rev
A3	Cyborg_TGL-H RTX	X01

Date: Friday, November 20, 2020 Sheet 56 of 106



https://vinafix.com

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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Display (DP Conn/Redriver / DVI)*

Size	Document Number	Rev
A3	Cyborg_TGL-H RTX	X01

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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Display (Backlight PWR)*

Size	Document Number	Rev
A3	Cyborg_TGL-H RTX	X01

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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *INT IO (HDD/ODD)*

Size	Document Number	Rev
A3	Cyborg_TGL-H RTX	X01

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Main Func = WLAN

17 WLAN_PCIE_RX_N
17 WLAN_PCIE_RX_P
17 WLAN_PCIE_TX_N
17 WLAN_PCIE_TX_P
19 WLAN_CLK_CPU_P
19 WLAN_CLK_CPU_N
20 WLAN_CLKREQ_CPU_N

18 BT_USB20_N
18 BT_USB20_P

21 PCIE_WAKE_N

20,26,63,71,79,91 PLT_RST_N

19 CNV_WR_DN1
19 CNV_WR_DP1
19 CNV_WR_DN0
19 CNV_WR_DP0
19 CNV_WR_CLKN
19 CNV_WR_CLKP
19 CNV_WT_DN1
19 CNV_WT_DP1
19 CNV_WT_DN0
19 CNV_WT_DP0
19 CNV_WT_CLKN
19 CNV_WT_CLKP
21 CNV_BRI_RSP
11,21 CNV_RGI_DT_CON
21 CNV_BRI_DT_CON
21 CNV_RGI_RSP
20 CNV_RF_RESET#

20 CLKREQ_CNV#

21 WLAN_WIGIG60GHZ_DIS#
20 BT_RADIO_DIS#

16,24 SUS_CLK

20 CNV_DET#

ARD:WLAN_WAKE>>BOM:Use R6106

3D3V_S5 — R6106 0R5J-5-GP — 3D3V_WLAN

C6101 SCD1U16V2KX-3DLGP
C6103 SCD1U16V2KX-3DLGP
C6104 SC22U6D3V3MX-1DLGP

R6111 0R2J-2-GP
EL6101 DY DLM0NSN900HY2D-GP
068.09002.2001
R6113 0R2J-2-GP

BT_USB20_P — BT_USB20_P_CON
BT_USB20_N — BT_USB20_N_CON

3D3V_WLAN
R6109 10KR2J-3-GP
WLAN_WIGIG60GHZ_DIS# — R6134 0R2J-2-GP — WLAN_WIGIG60GHZ_DIS#_R

3D3V_WLAN
R6110 10KR2J-3-GP
R6133 DY 0R2J-2-GP
BT_RADIO_DIS# — RB520S30-GP — D6102 — BT_RADIO_DIS#_R

83.R2003.A8M
2ND = 083.52030.008F

3D3V_WLAN
PCIE_WAKE_N — R6117 DY 10KR2J-3-GP

1090mA

WLAN1
SKT-NGFF75P-164-GP
062.10003.0B11

NP1		NP2	
	1		2
GND	3	3_3VAUX	4
USB_D+	5	3_3VAUX	6
USB_D-	7	LED#1	8
GND	9	PCM_CLK	10
SDIO_CLK	11	PCM_SYNC	12
SDIO_CMD	13	PCM_IN	14
SDIO_DAT0	15	PCM_OUT	16
SDIO_DAT1	17	LED#2	18
SDIO_DAT2	19	GND	20
SDIO_DAT3	21	UART_WAKE	22
SDIO_WAKE	23	UART_RX	
SDIO_RESET			
	33	UART_TX	32
GND	35	UART_RTS	34
PETP0	37	UART_CTS	36
PETN0	39	CLINK_RESET	38
GND	41	CLINK_DATA	40
PERP0	43	CLINK_CLK	42
PERN0	45	COEX3	44
GND	47	COEX2	46
REFCLKP0	49	COEX1	48
REFCLKN0	51	SUSCLK_32KHZ	50
GND	53	PERST0#	52
CLKREQ0#	55	RESERVED#54/W_DISABLE#2	54
PEWAKE0#	57	W_DISABLE#1	56
GND	59	NFC_I2C_SM_DATA	58
RESERVED#59/2ND_LANE_PETP1	61	NFC_I2C_SM_CLK	60
RESERVED#61/2ND_LANE_PETN1	63	NFC_I2C_IRQ/MGPIO5	62
GND	65	GPIO0_NFC_RESET#/MGPIO7	64
RESERVED#65/2ND_LANE_PERP1	67	RESERVED#66	66
RESERVED#67/2ND_LANE_PERN1	69	RESERVED#68	68
GND	71	RESERVED#70	70
RESERVED#71	73	3_3VAUX	72
RESERVED#73	75	3_3VAUX	74
GND	77	76	

BT_USB20_P_CON
BT_USB20_N_CON

CNV_WR_DN1 R6114 0R2J-2-GP — CNV_WR_DN1_R
CNV_WR_DP1 R6115 0R2J-2-GP — CNV_WR_DP1_R
CNV_WR_DN0 R6116 0R2J-2-GP — CNV_WR_DN0_R
CNV_WR_DP0 R6118 0R2J-2-GP — CNV_WR_DP0_R
CNV_WR_CLKN R6119 0R2J-2-GP — CNV_WR_CLKN_R
CNV_WR_CLKP R6120 0R2J-2-GP — CNV_WR_CLKP_R

WLAN_PCIE_TX_P C6115 SCD1U16V2KX-3DLGP — WLAN_PCIE_TX_P_C
WLAN_PCIE_TX_N C6102 SCD1U16V2KX-3DLGP — WLAN_PCIE_TX_N_C

WLAN_PCIE_RX_P
WLAN_PCIE_RX_N
WLAN_CLK_CPU_P
WLAN_CLK_CPU_N
WLAN_CLKREQ_CPU_N
PCIE_WAKE_N

CNV_WT_DN1 R6121 0R2J-2-GP — CNV_WT_DN1_R
CNV_WT_DP1 R6122 0R2J-2-GP — CNV_WT_DP1_R
CNV_WT_DN0 R6123 0R2J-2-GP — CNV_WT_DN0_R
CNV_WT_DP0 R6124 0R2J-2-GP — CNV_WT_DP0_R
CNV_WT_CLKN R6125 0R2J-2-GP — CNV_WT_CLKN_R
CNV_WT_CLKP R6126 0R2J-2-GP — CNV_WT_CLKP_R

3D3V_WLAN
EC6101 DY SCD01U50V2KX-1DLGP
R6132 DY 0R2J-2-GP — CNV_DET#
CNV_RF_RESET#
CLKREQ_CNV#
CNV_BRI_RSP_R — R6127 49D9R2F-GP — CNV_BRI_RSP
CNV_RGI_DT_CON
CNV_RGI_RSP_R — R6112 49D9R2F-GP — CNV_RGI_RSP
CNV_BRI_DT_CON
SUS_CLK_WLAN — R6135 33R2J-2-GP — SUS_CLK
WLAN_RST# — R6131 0R2J-2-GP — PLT_RST_N
BT_RADIO_DIS#_R
WLAN_WIGIG60GHZ_DIS#_R
PULSAR_38P4M_REFCLK — TP6101
3D3V_WLAN

2017.10.16
Andy share CNV_DET connect to CNV_RST PIN .
Need to confirm Hi det/low det to ph/pl

CNV_RF_RESET# — R6101 75KR2F-GP
CLKREQ_CNV# — R6102 75KR2F-GP
DY

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Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (WLAN M.2)
Size: Custom
Document Number: Cyborg_TGL-H RTX
Rev: X01
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SSID = Wireless

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Title: INT IO (RSVD) WWAN

Size	Document Number	Rev
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Date: Friday, November 20, 2020 Sheet 62 of 106

Mini Card Connector (NGFF m-SATA)

SSID = m-SATA

Important! SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

20,26,61,71,79,91 PLT_RST_N
64 M2_PCIE_LED#
24 SSD_SCP#
21 PCH_SSD_RST_N
21 M2_SSD2_PEDET
21 mSATA_DEVSLP2

SSD1

19 SSD_CLK_CPU_P
19 SSD_CLK_CPU_N
20 SSD_CLKREQ_CPU_N
3 SSD_PCIE_TX_P4
3 SSD_PCIE_TX_N4
3 SSD_PCIE_RX_P4
3 SSD_PCIE_RX_N4
3 SSD_PCIE_TX_P3
3 SSD_PCIE_TX_N3
3 SSD_PCIE_RX_P3
3 SSD_PCIE_RX_N3
3 SSD_PCIE_TX_P2
3 SSD_PCIE_TX_N2
3 SSD_PCIE_RX_P2
3 SSD_PCIE_RX_N2
3 SSD_PCIE_TX_P1
3 SSD_PCIE_TX_N1
3 SSD_PCIE_RX_P1
3 SSD_PCIE_RX_N1

SSD2

19 SSD2_CLK_CPU_P
19 SSD2_CLK_CPU_N
20,21 SSD2_CLKREQ_CPU_N
17 SSD2_PCIE_RX_N1
17 SSD2_PCIE_RX_P1
17 SSD2_PCIE_TX_N1
17 SSD2_PCIE_TX_P1
17 SSD2_PCIE_RX_N2
17 SSD2_PCIE_RX_P2
17 SSD2_PCIE_TX_N2
17 SSD2_PCIE_TX_P2
17 SSD2_PCIE_RX_N3
17 SSD2_PCIE_RX_P3
17 SSD2_PCIE_TX_N3
17 SSD2_PCIE_TX_P3
17 SSD2_SATA_RX_N4
17 SSD2_SATA_RX_P4
17 SSD2_SATA_TX_N4
17 SSD2_SATA_TX_P4

3D3V_S0 — R6355 1Ω D01R5F-GP — 3D3V_SSD1

Current Sense R

C6305 SC33P50V2JN-3DLGP
C6304 SC33P50V2JN-3DLGP
C6306 SCD047U25Y2KX-4-GP
C6308 SCD047U25Y2KX-4-GP
C6307 SCD1U25V2KX-1-DL-GP
C6317 SC220UED0J3MX-1-DL-GP
C6318 SC220UED0J3MX-1-DL-GP
DY FC6301 SC15P50V2JN-DL-GP

11/10 Add

R6315 1 DY 0R1J-GP — 3D3V_S5_PCH

C6332 SCD1U16V1KX-5-GP

U6301 TC7SZ08FU-LJ-CY-GP
073.7SZ08.000G

PLT_RST_N
PCH_SSD_RST_N
PLT_RST__SSD1_N

R6314 100KR1J-GP

SSD M.2 CONN_2nd

SSD1 — SKT-NGFF75P-224-GP
062.10003.0F31

3D3V_SSD1 — R6305 10KR2J-3-GP

M2_SSD_PEDET
SSD_CLKREQ_CPU_N
PLT_RST__SSD1_N — R6308 0R2J-2-GP — MSATA_RST#
MSATA_DEVSLP1 — AFTP6307 AFTE14P-1-GP
M2_PCIE_LED# — R6307 0R2J-2-GP — M2_PCIE_LED#_R
SSD_SCP#_R
PEDET(OC_PCIE/GND_SATA)
D_PERP0/SATA_A+/H_PETP0
D_PERN0/SATA_A-/H_PETN0
D_PETP0/SATA_B-/H_PERP0
D_PETN0/SATA_B+/H_PERN0
D_PERP1/H_PETP1
D_PERN1/H_PETN1
D_PETP1/H_PERP1
D_PETN1/H_PERN1
D_PERP2/H_PETP2
D_PERN2/H_PETN2
D_PETN2/H_PERP2
D_PETP2/H_PERN2
D_PERP3/H_PETP3
D_PERN3/H_PETN3
D_PETN3/H_PERP3
D_PETP3/H_PERN3

SSD_PCIE_TX_C_P4 C6302 1 — SCD22U10V2KX-1GP — SSD_PCIE_TX_P4
SSD_PCIE_TX_C_N4 C6303 1 — SCD22U10V2KX-1GP — SSD_PCIE_TX_N4
SSD_PCIE_TX_C_P3 C6311 1 — SCD22U10V2KX-1GP — SSD_PCIE_TX_P3
SSD_PCIE_TX_C_N3 C6312 1 — SCD22U10V2KX-1GP — SSD_PCIE_TX_N3
SSD_PCIE_TX_C_P2 C6313 1 — SCD22U10V2KX-1GP — SSD_PCIE_TX_P2
SSD_PCIE_TX_C_N2 C6314 1 — SCD22U10V2KX-1GP — SSD_PCIE_TX_N2
SSD_PCIE_TX_C_P1 C6315 1 — SCD22U10V2KX-1GP — SSD_PCIE_TX_P1
SSD_PCIE_TX_C_N1 C6316 1 — SCD22U10V2KX-1GP — SSD_PCIE_TX_N1

SSD_CLK_CPU_P
SSD_CLK_CPU_N
SSD_PCIE_RX_P4
SSD_PCIE_RX_N4
SSD_PCIE_RX_P3
SSD_PCIE_RX_N3
SSD_PCIE_RX_P2
SSD_PCIE_RX_N2
SSD_PCIE_RX_P1
SSD_PCIE_RX_N1

3D3V_SSD1 — AFTP6304 AFTE14P-1-GP

3D3V_S0 — R6309 100KR2J-1-GP DY — SSD_SCP# — R6305 0R2J-2-GP — SSD_SCP#_R

3D3V_SSD2 — R6303 10KR2J-3-GP DY — mSATA_DEVSLP2 — R6304 10KR2J-3-GP DY

3D3V_S0 — R6356 1Ω D01R5F-GP — 3D3V_SSD2

Current Sense R

C6310 SC33P50V2JN-3DLGP
C6309 SC33P50V2JN-3DLGP
C6319 SCD047U25Y2KX-4-GP
C6320 SCD047U25Y2KX-4-GP
C6321 SCD1U25V2KX-1-DL-GP
C6322 SC22U6D3Y3MX-1-DL-GP
C6323 SC22U6D3Y3MX-1-DL-GP
DY FC6302 SC15P50V2JN-DL-GP

SSD M.2 CONN_Main

SSD2 — SKT-NGFF75P-224-GP
062.10003.0F31

3D3V_SSD2 — R6311 10KR2J-3-GP

M2_SSD2_PEDET
SSD2_CLKREQ_CPU_N
PLT_RST_N — R6310 0R2J-2-GP — MSATA_RST2#
mSATA_DEVSLP2 — R6313 0R2J-2-GP — MSATA_DEVSLP2_R
M2_PCIE_LED# — R6312 0R2J-2-GP — M2_PCIE_LED#_R2
SSD_SCP#_R
PEDET(OC_PCIE/GND_SATA)
D_PERP0/SATA_A+/H_PETP0
D_PERN0/SATA_A-/H_PETN0
D_PETP0/SATA_B-/H_PERP0
D_PETN0/SATA_B+/H_PERN0
D_PERP1/H_PETP1
D_PERN1/H_PETN1
D_PETP1/H_PERP1
D_PETN1/H_PERN1
D_PERP2/H_PETP2
D_PERN2/H_PETN2
D_PETN2/H_PERP2
D_PETP2/H_PERN2
D_PERP3/H_PETP3
D_PERN3/H_PETN3
D_PETN3/H_PERP3
D_PETP3/H_PERN3

SSD2_SATA_TX_C_P4 C6324 1 — SCD22U10V2KX-1GP — SSD2_SATA_TX_P4
SSD2_SATA_TX_C_N4 C6325 1 — SCD22U10V2KX-1GP — SSD2_SATA_TX_N4
SSD2_PCIE_TX_C_P3 C6327 1 — SCD22U10V2KX-1GP — SSD2_PCIE_TX_P3
SSD2_PCIE_TX_C_N3 C6326 1 — SCD22U10V2KX-1GP — SSD2_PCIE_TX_N3
SSD2_PCIE_TX_C_P2 C6328 1 — SCD22U10V2KX-1GP — SSD2_PCIE_TX_P2
SSD2_PCIE_TX_C_N2 C6329 1 — SCD22U10V2KX-1GP — SSD2_PCIE_TX_N2
SSD2_PCIE_TX_C_P1 C6330 1 — SCD22U10V2KX-1GP — SSD2_PCIE_TX_P1
SSD2_PCIE_TX_C_N1 C6331 1 — SCD22U10V2KX-1GP — SSD2_PCIE_TX_N1

SSD2_SATA_RX_N4
SSD2_SATA_RX_P4
SSD2_PCIE_RX_N3
SSD2_PCIE_RX_P3
SSD2_PCIE_RX_N2
SSD2_PCIE_RX_P2
SSD2_PCIE_RX_N1
SSD2_PCIE_RX_P1

3D3V_SSD2 — AFTP6306 AFTE14P-1-GP

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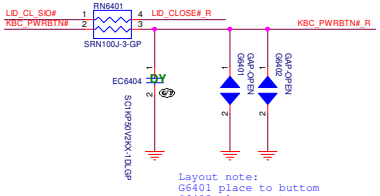
Title: INT IO (SSD M.2/ eMMC)

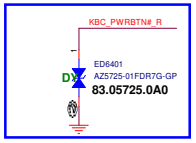
Size: Custom | Document Number: Cyborg_TGL-H RTX | Rev: X01

Date: Friday, November 20, 2020 | Sheet 63 of 106

Main Func = Power BTN

close to IOBD1



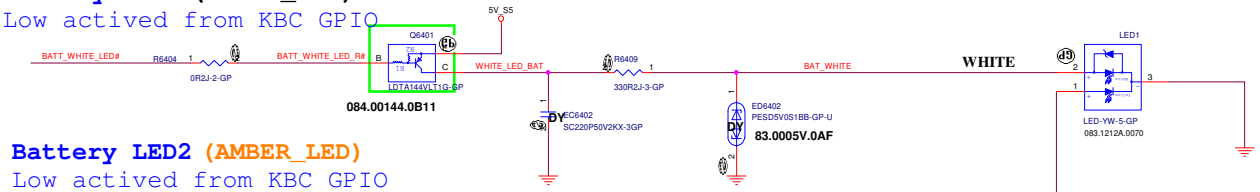


0614 Layout HT

24,66 LID_CL_SIO#
24,64 KBC_PWRBTN#
66 KBC_PWRBTN#_R
66,67 LID_CLOSE#_R

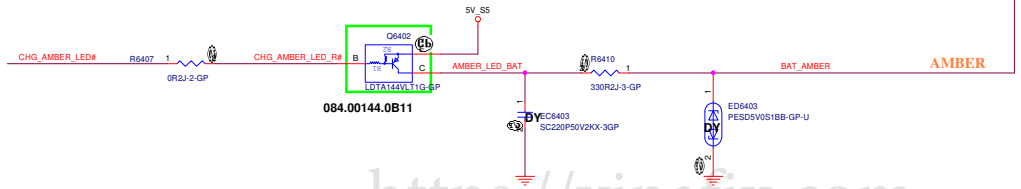
Battery LED1 (WHITE_LED)

Low actived from KBC GPIO



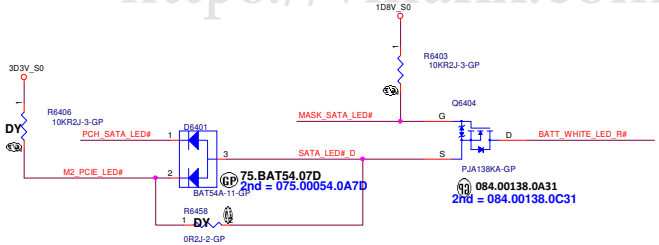
Battery LED2 (AMBER_LED)

Low actived from KBC GPIO



24 BATT_WHITE_LED#
21 PCH_SATA_LED#
24 MASK_SATA_LED#
63 M2_PCIE_LED#

SATA LED

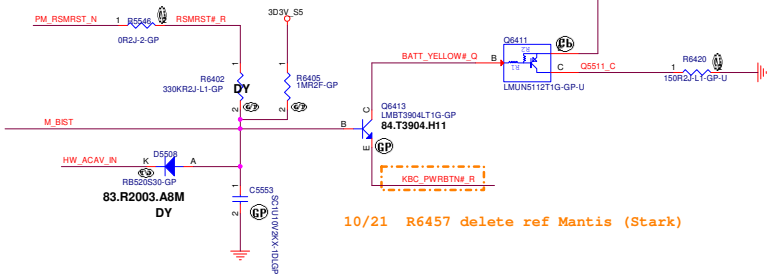


17 PM_RSMRST_N
24,44 HW_ACAV_IN
24,64 KBC_PWRBTN#

KBC

24 M_BIST
24 CHG_AMBER_LED#

M-BIST for G10 (Proposed schematic)
follow bandon



10/21 R6457 delete ref Mantis (Stark)

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TGL-H

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LED / Button / Power Button

Size: A2 | Document Number: Cyborg_TGL-H RTX | Rev: X01

Date: Friday, November 20, 2020 | Sheet 64 of 106

Main Func = Keyboard

KB Backlight Power Consumption: 285mA max.

5V_S0 → F6502 POLYSW-1D1A6V-9-GP-U → +5V_KB_BL

69.48001.081
2nd = 69.50011.081

C6501 SCD1U25V2KX-1-DL-GP

X01 20161228 change

+5V_KB_BL, KB_LED_DET_C, KB_BL_CTRL# → KBBL1 ACES-CON4-90-GP-U

020.K0298.0004
2nd = 020.K0311.0004

Change ESD 2KV

24 KB_LED_PWM → R6509 100KR2J-1-GP → Q6501 PJA138KA-GP → KB_BL_CTRL#

084.00138.0A31
2nd = 084.00138.0C31

21 KB_BL_DET → R6507 51KR2J-1-GP → KB_LED_DET_C

R6508 100KR2J-1-GP, C6504 SCD1U16V2KX-3GP

+5V_KB_BL → AFTP6529 AFTE14P-1-GP

KB_BL_CTRL# → AFTP6530 AFTE14P-1-GP

X02 0414

24 CAP_LED#_R → R6512 2 → CAP_LED_R# → Q6505 LDTA144VLT1G-GP (C, B, E) → CAP_LED_Q → R6513 1KR2J-1-GP → CAP_LED

5V_S5

CAP_LED_Q → EC6507 SCD1U16V2KX-4GP

short pad change 0 ohm

084.00144.0B11

CAP LED Control
LOW actived from KBC GPIO

24 KSI[0..7] → KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7

24 KSO[00..16] → KSO00 KSO01 KSO02 KSO03 KSO04 KSO05 KSO06 KSO07 KSO08 KSO09 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15 KSO16

20 KB_DET# → AFTP6542 … AFTP6566 (AFTE14P-1-GP) → KB1 PTWO-CON30-18-GP

020.K0210.0030
2nd = 020.K0236.0030

Main Func = TPAD

24 PTP_DIS#

TP_VDD

3D3V_S5_PCH → R6514 1 0R3J-0-U-GP → TP_VDD

R6557 10KR2J-3-GP

PTP_DIS# → D6501 RB520S30-GP (K, A) → PTP_CON_DIS#

83.R2003.A8M
2ND = 083.52030.008F

ARD:TP_WAKE>>BOM:Use R6514

RN6503 SRN2K2J-1-GP

020.K0255.0008
PTWO-CON8-18-GP

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

EC I2C

I2C

24,57 DAT_TP_SIO_I2C_CLK → R6515 0R2J-2-GP → CPU_I2C_SCL_TP
24,57 CLK_TP_SIO_I2C_DAT → R6516 0R2J-2-GP → CPU_I2C_SDA_TP

20,66 CPU_I2C_SCL_P1 → R6505 0R2J-2-GP → CPU_I2C_SCL_TP
20,66 CPU_I2C_SDA_P1 → R6506 0R2J-2-GP → CPU_I2C_SDA_TP

EC6501 SC33P50V2JN-3GP

C4347 SC1KP50V2KX-1DLGP, C4348 SC1KP50V2KX-1DLGP

Placement: Close to TPAD1

C6505 SCD1U25V2KX-1-DL-GP

21,24 TOUCHPAD_INTR# → CPU_I2C_SDA_TP, CPU_I2C_SCL_TP, PTP_CON_DIS# → TPAD1

AFTE14P-1-GP AFTP6540

Change pindefine DVT1 0210 1330

Need to check if it is Active High or Active Low
and check if there is PH on TPAD side.

X02 0415

TP_VDD → R6511 10KR2J-3-GP → TOUCHPAD_INTR#

TP_VDD → AFTP6531
CPU_I2C_SCL_TP → AFTP6534
CPU_I2C_SDA_TP → AFTP6535
TOUCHPAD_INTR# → AFTP6536
PTP_DIS# → AFTP6537

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TGL-H

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21F, 88, Sec 1 Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (KB/TP)

Size: Custom | Document Number: Cyborg_TGL-H RTX | Rev: X01

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USB3.1

18 USB3_USB30_TX_N
18 USB3_USB30_TX_P
18 USB3_USB30_RX_N
18 USB3_USB30_RX_P

18 USB3_USB20_P
18 USB3_USB20_N

USB Power

20200206 USB_OC1_N

FP

24 FPR_SCAN#
64 KBC_PWRBTN#_R
18 FP1_USB20_N
18 FP1_USB20_P

16,51 PM_SLP_S4#

21 SD_READ_MODE#

18 CARD1_USB20_N
18 CARD1_USB20_P

20,65 CPU_I2C_SCL_P1
20,65 CPU_I2C_SDA_P1

44 BT_PWR_IN-
44 BT_PWR_IN+

AUDIO

27 AUD_SENSE
29 AUD_HP1_JACK_L1
29 AUD_HP1_JACK_R1
27,29 AUD_RING
27,29 AUD_SLEEVE

LID

24 LID_POWER_ON#
24,64 LID_CL_SIO#
67 LID_CL_NB#

64,67 LID_CLOSE#_R

AUDIO

10/22 IOBD1.18 PW 3D3V_S0

FOR FPR

KBC_PWRBTN#_R R6613 1 2 2R2J-2-GP
FPR_SCAN# 1 R6614 2 2R2J-2-GP

07/21 Hall1 Change to MB

IOBD1

AUD_AGND
AUD_HP1_JACK_L1
AUD_RING
AUD_RING
AUD_RING
AUD_SLEEVE
AUD_SLEEVE
AUD_HP1_JACK_R1
AUD_SENSE
USB30_VCCB
3D3V_S5
PM_SLP_S4#
FPR_SSO_SW#
FPR_SCAN#_H
SD_READ_MODE#
LID_CLOSE#_R
FP1_USB20_P
FP1_USB20_N
USB3_USB20_CON_P
USB3_USB20_CON_N
CARD1_USB20_CON_N
CARD1_USB20_CON_P
USB3_USB30_RX_P
USB3_USB30_RX_N
USB3_USB30_TX_P
USB3_USB30_TX_N

STAR-CON40-8-GP
020.F0847.0040

10/17 IOBD1.37 connect to GND (Stark)
10/17 IOBD1.18 change from BREATH_LED# to 3D3V_S0(Stark)

R6601 DY 0R2J-2-GP
EL6601 DLM0NSN900HY2D-GP 068.09002.2001
R6602 DY 0R2J-2-GP
USB3_USB20_P
USB3_USB20_N
USB3_USB20_CON_P
USB3_USB20_CON_N

R6603 DY 0R2J-2-GP
EL6603 DLM0NSN900HY2D-GP 068.09002.2001
R6604 DY 0R2J-2-GP
CARD1_USB20_P
CARD1_USB20_N
CARD1_USB20_CON_P
CARD1_USB20_CON_N

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E3 reserve E3 stuff until PVT

CN1 HRS-CONN20A-2-GP 20.F1450.020

IN1+ 3D3V_S5 3D3V_WLAN
IN1- R6635 E3 0R1J-GP 19V_DCBATOUT_E3_1
IN2+ 3D3V_S0 3D3V_SSD2
IN2- R6617 E3 0R1J-GP PWR_DCBATOUT_VCCGT_E3
R6618 E3 0R1J-GP 3D3V_S0_H_E3
R6619 E3 0R1J-GP 3D3V_SSD2_E3
CPU_I2C_SCL_P1 R6620 E3 0R1J-GP CPU_I2C_SCL_P1_E3
IN7- R6622 E3 0R1J-GP PWR_DCBATOUT_VDDQ
IN7+ R6624 E3 0R1J-GP 19V_DCBATOUT_E3_2
IN8- R6623 E3 0R1J-GP PWR_DCBATOUT_VCCSA_E3
IN8+ R6634 E3 0R1J-GP 19V_DCBATOUT_E3_3

R0201 Please to close power source

19V_DCBATOUT_E3_4
DCBATOUT_LCD_R_E3
3D3V_LCDVDD_H_E3
3D3V_LCDVDD_S0_E3
CPU_I2C_SDA_P1_E3
3D3V_S0_E3
PWR_DCBATOUT_VCCCORE_E3
19V_DCBATOUT_E3_5
BT_PWR_IN-
BT_PWR_IN+

R6636 E3 0R1J-GP 19V_DCBATOUT
R6625 E3 0R1J-GP DCBATOUT_LCD_R
R6626 E3 0R1J-GP 3D3V_LCDVDD_R
R6628 E3 0R1J-GP 3D3V_LCDVDD_S0
R6627 E3 0R1J-GP CPU_I2C_SDA_P1
R6629 E3 0R1J-GP 3D3V_S0
R6630 E3 0R1J-GP PWR_DCBATOUT_VCCCORE
R6632 E3 0R1J-GP 19V_DCBATOUT

IN4+ LCD BACKLIGHT
IN4- IN3+ Panel logic power IN3-
IN6- IN6+ 1V_CPU_CORE input
IN5- IN5+ System power source

LID sensor

R6639 1 DY 0R2J-2-GP
LID_CL_SIO# A D6601 RB520S30-GP LID_CL_NB#
83.R2003.A8M
2ND = 083.52030.008F

LID_POWER_ON# R6637 1MR2J-1-GP Q6701_G
C6604 SCD1U16V2KX-3DLGP
Q6601 2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
R6638 680KR2F-GP 3D3V_AUX_S5
C6606 SCD1U16V2KX-3DLGP
C6603 SC1U10V2KX-1DLGP
D6602 A RB520S30-GP Q6701_G_D
83.R2003.A8M
2ND = 083.52030.008F

For IO USB2.0 port use

5V_S5 C6625 SC1U10V2KX-1DLGP
USB_PWR_EN#
U6603 SY6288DAAC-GP
IN EN# OUT GND OC#
074.06288.009B
2ND = 074.03553.007G
USB30_VCCB
C6627 SCD1U16V2KX-3DLGP
C6626 SC1U25V3KX-1DLGP
USB_OC1_N 20200206

Close to IOBD1

TGL-H

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

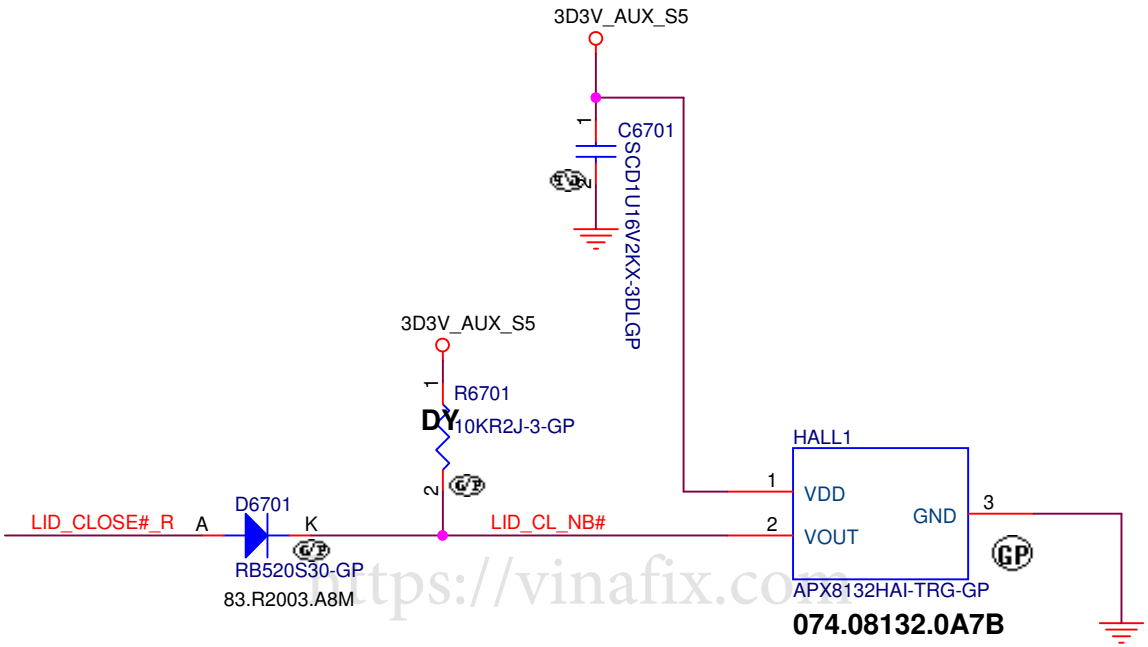
Title: IO Board Conn (USB/AUDIO/CR..etc)

Size: Custom | Document Number: Cyborg_TGL-H RTX | Rev: X01

Date: Friday, November 20, 2020 | Sheet 66 of 106

64,66 LID_CLOSE#_R

66 LID_CL_NB#



https://vinafix.com

TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Sensor (Hall-Sensor)***

Size	Document Number	Rev
A	Cyborg_TGL-H RTX	X01

Date: Friday, November 20, 2020 Sheet 67 of 106

Main Func = Debug

20 ESPI_CPU_IO0_DBG
20 ESPI_CPU_IO1_DBG
20 ESPI_CPU_IO2_DBG
20 ESPI_CPU_IO3_DBG
20 ESPI_CPU_CLK_DBG
20,24 ESPI_CPU_CS_N
20,24 ESPI_CPU_RST_N

20 UART_2_CTXD_DRXD
20 UART_2_CRXD_DTXD

20200206

20200206

ESPI_CPU_CLK_DBG
ESPI_CPU_RST_N
ESPI_CPU_CS_N
ESPI_CPU_IO3_DBG
ESPI_CPU_IO2_DBG
ESPI_CPU_IO1_DBG
ESPI_CPU_IO0_DBG

Debug Connector

DBG1
15
1
2
3
4
5
6
7
8
9
10
11
12
13
14
16
zz.F0765.01401
DY
GP
ACES-CON14-5-GP

20.F0765.014

X01 20161223 change

3D3V_S0

24 HOST_DEBUG_TX
R6801 1 DY 2 0R2J-2-GP HOST_DEBUG_TX_CON

UART_2_CRXD_DTXD
R6803 1 DEBUG 0R2J-2-GP UART_2_CRXD_DTXD_CON

UART_2_CTXD_DRXD
R6802 1 DEBUG 0R2J-2-GP UART_2_CTXD_DRXD_CON

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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Debug (LPC debug)

Size: Custom
Document Number: Cyborg_TGL-H RTX
Rev: X01

Date: Friday, November 20, 2020
Sheet 68 of 106

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TGL-H

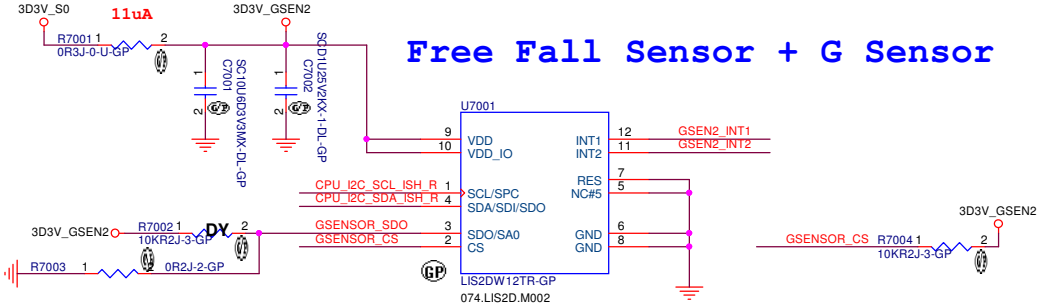
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Sensor (RSVD)***		
Size: A4	Document Number: **Cyborg_TGL-H RTX**	Rev: **X01**
Date: Friday, November 20, 2020	Sheet 69 of 106	

SSID = Free Fall Sensor

21 GSEN2_INT1_C
21 GSEN2_INT2_C

20 CPU_I2C_SDA_ISH
20 CPU_I2C_SCL_ISH

Free Fall Sensor + G Sensor

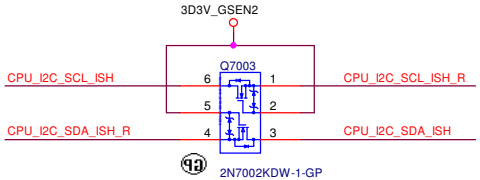


pch
1.8V_S5

GSEN2_INT1_C R7005 1 0R2J-2-GP GSEN2_INT1
GSEN2_INT2_C R7006 1 0R2J-2-GP GSEN2_INT2

3.3V_S0

https://vinafix.com



75.27002.F7C
2nd = 075.67002.007C
3rd = 075.063D1.007C

CPU

3.3V_S5

CPU_I2C_SCL_ISH R7007 1 DY 0R2J-2-GP CPU_I2C_SCL_ISH_R
CPU_I2C_SDA_ISH R7009 1 DY 0R2J-2-GP CPU_I2C_SDA_ISH_R

3.3V_S0

3D3V_GSEN2
R7045 10KR2J-3-GP
R7044 10KR2J-3-GP

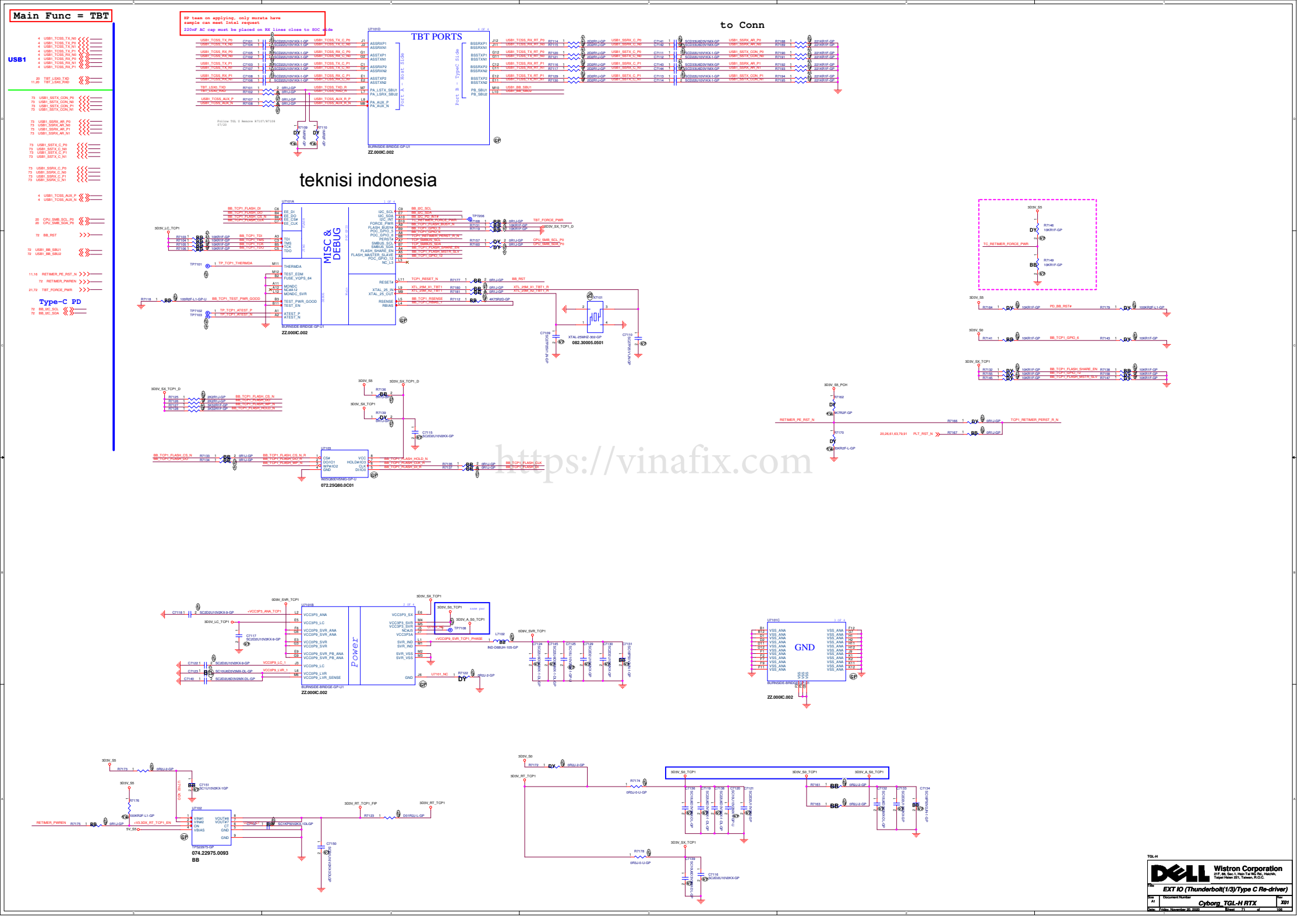
TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sensor (G-sensor)

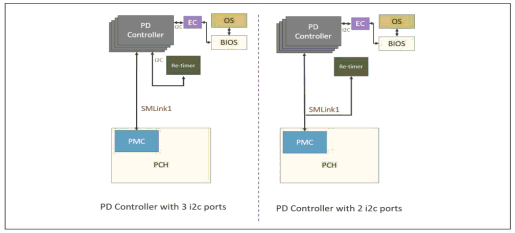
Size	Document Number	Rev
Custom	Cyborg_TGL-H RTX	X01

Date: Friday, November 20, 2020 Sheet 70 of 106


Main Func = TBT
HP team on applying, only murata have sample can meet Intel request
220nF AC cap must be placed on RX lines close to SOC side
to Conn
TBT PORTS
USB1
Type-C PD
MISC & DEBUG
Power
GND
teknisi indonesia
https://vinafix.com
ZZ.000IC.002
074.22975.0093
072.25Q80.0C01
082.30005.0501
Wistron Corporation
EXT IO (Thunderbolt(1/3)/Type C Re-driver)
Cyborg_TGL-H RTX
Friday, November 20, 2020

Main Func = TypeC

Figure 87. SMBus / SMlink Connectivity for USB Type-C PD Controller



Type-C PD

PD to SOC

PD to EC

PD to BB

PD to EC

CCG5's I2C address is decided by the SWD clock pin.
Don't mount R8 and R9 for the I2C address 0x08. This is the default one.
Mount only R9 for the I2C address 0x40.
Mount only R8 for the I2C address 0x42.

ID1

ID2

	Dell TGL Platform MOD_ID Options NEW		
Project	MOD_ID1	MOD_ID2	Description
Cyborg-TGL-H	L3	L2	TGL-H/BB8040/CCG6SF

	CCG6_ID	R7216	R7218	計算值	理論值
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1	064.71535.06D1 (715K)	64.10035.6DL (100K)	0.123	0.125
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5	0.5
5/8	L5	64.10035.6DL (100K)	64.20035.6DL (200K)	0.625	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728	0.75
7/8	L7	64.10035.6DL (100K)	064.71535.06D1 (715K)	0.877	0.875

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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (Thunderbolt(2/3)/Type C CC Logic)

Size: A2 | Document Number: Cyborg_TGL-H RTX | Rev: X01

Date: Friday, November 20, 2020 | Sheet 72 of 106

Main Func = TypeC

USB1

71 USB1_SSTX_CON_P0
71 USB1_SSTX_CON_N0
71 USB1_SSTX_CON_P1
71 USB1_SSTX_CON_N1

71 USB1_SSRX_AR_P0
71 USB1_SSRX_AR_N0
71 USB1_SSRX_AR_P1
71 USB1_SSRX_AR_N1

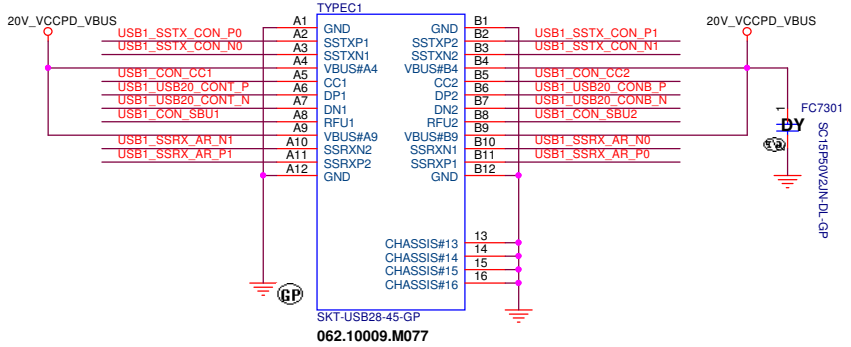
72 USB1_USB20_CMCT_P
72 USB1_USB20_CMCT_N
72 USB1_USB20_CMCB_P
72 USB1_USB20_CMCB_N

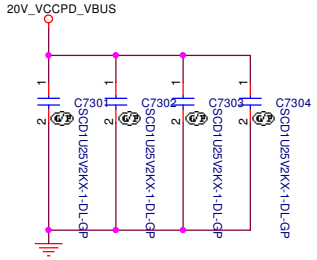
72 USB1_CON_CC1
72 USB1_CON_CC2

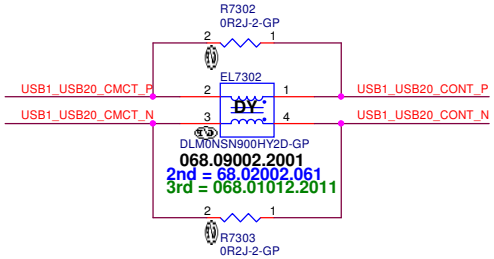
72 USB1_CON_SBU1
72 USB1_CON_SBU2

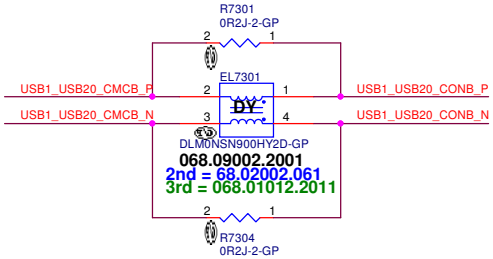
71 USB1_SSTX_C_P0
71 USB1_SSTX_C_N0
71 USB1_SSTX_C_P1
71 USB1_SSTX_C_N1

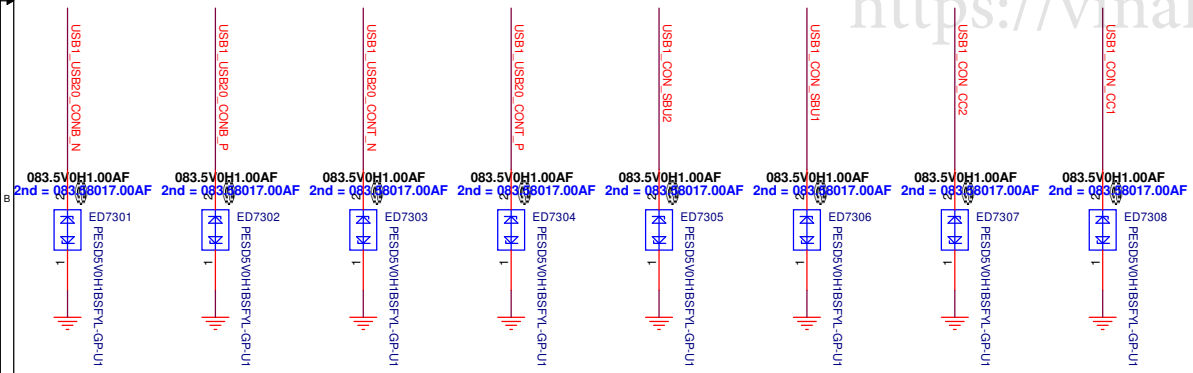
71 USB1_SSRX_C_P0
71 USB1_SSRX_C_N0
71 USB1_SSRX_C_P1
71 USB1_SSRX_C_N1

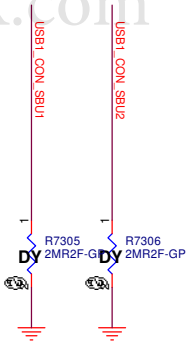


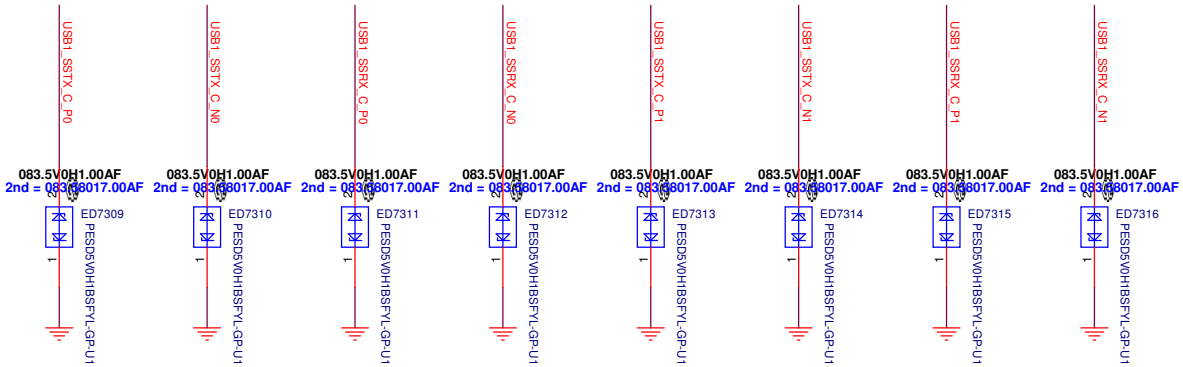












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TGL-H

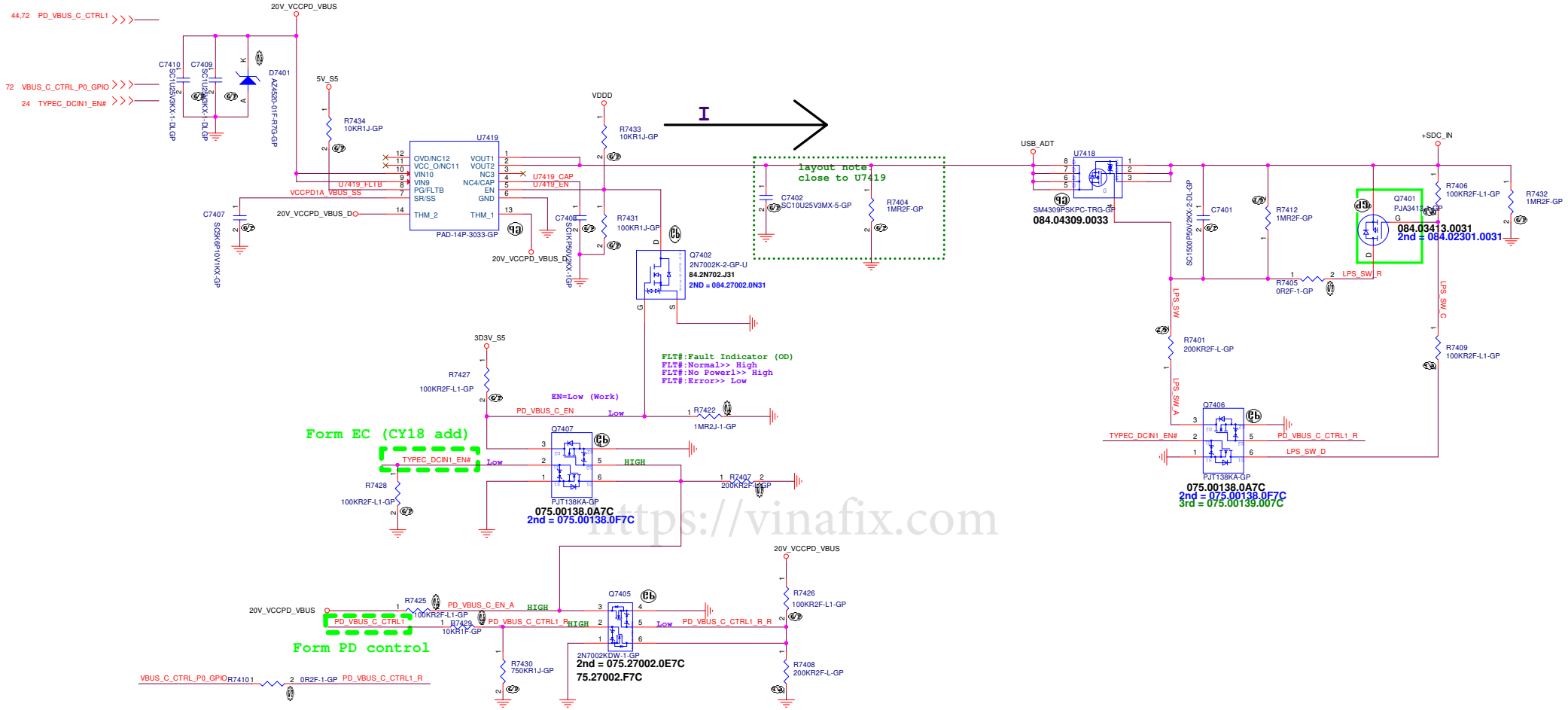
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (Thunderbolt(3/3)/Type C Conn)

Size	Document Number	Rev
A3	Cyborg_TGL-H RTX	X01

Date: Friday, November 20, 2020 Sheet 73 of 106

Main FUNC = LPS



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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (TYPEC Power delivery/VBUS)

Size	Document Number	Rev
Custom	Cyborg_TGL-H RTX	X01

Date: Friday, November 20, 2020 Sheet 74 of 106

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TGL-H

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *EXT IO (RSVD)*

Size	Document Number	Rev
A3	Cyborg_TGL-H RTX	X01

Date: Friday, November 20, 2020 Sheet 75 of 106

EMI Reserved

VGA_RST#

EC7601 0Y 0.01UF-25V-K-X7R-2-GP

20,24,86 DGPU_PWROK
21,76 CLK_PCIE_PEG_REQ#
79 VGA_RST#
19 GFX_CLK_CPU_P
19 GFX_CLK_CPU_N
21,76 CLK_PCIE_PEG_REQ#

3 GFX_PCIE_RX_P0
3 GFX_PCIE_RX_N0
3 GFX_PCIE_TX_CON_P0
3 GFX_PCIE_TX_CON_N0
3 GFX_PCIE_RX_P1
3 GFX_PCIE_RX_N1
3 GFX_PCIE_TX_CON_P1
3 GFX_PCIE_TX_CON_N1
3 GFX_PCIE_RX_P2
3 GFX_PCIE_RX_N2
3 GFX_PCIE_TX_CON_P2
3 GFX_PCIE_TX_CON_N2
3 GFX_PCIE_RX_P3
3 GFX_PCIE_RX_N3
3 GFX_PCIE_TX_CON_P3
3 GFX_PCIE_TX_CON_N3
3 GFX_PCIE_RX_P4
3 GFX_PCIE_RX_N4
3 GFX_PCIE_TX_CON_P4
3 GFX_PCIE_TX_CON_N4
3 GFX_PCIE_RX_P5
3 GFX_PCIE_RX_N5
3 GFX_PCIE_TX_CON_P5
3 GFX_PCIE_TX_CON_N5
3 GFX_PCIE_RX_P6
3 GFX_PCIE_RX_N6
3 GFX_PCIE_TX_CON_P6
3 GFX_PCIE_TX_CON_N6
3 GFX_PCIE_RX_P7
3 GFX_PCIE_RX_N7
3 GFX_PCIE_TX_CON_P7
3 GFX_PCIE_TX_CON_N7

DG-09845-001_v01 P.128

PEX_CLKREQ# is an active-low, open-drain bi-directional signal. It must have a 10 k pull-up to 1V8. For more details, refer to the Notebook PCIe Reference Clock Power-Down Feature Application Note (DA-05258-001.pdf).

DG-09845-001_v02 P.46

Rail (GPU Ball Name)	Balls	Voltage	Filtering under GPU	Filtering near GPU
PEX_DVDD_x [x=1-12] PEX_CVDD_x [x=1-3]	12	0.95V	6 x 1uF (0402 or 0201W X6S) 2 x 4.7uF (0603 X6S)	3 x 10uF (0805) 2 x 22uF (0805)
PEX_HVDD_x [x=1-13] PEX_PLL_HVDD	13 1	1.8V	9 x 1uF (0402 or 0201W X6S) 2 x 4.7uF (0603 X6S)	3 x 10uF (0805) 2 x 22uF (0805)

DGPU_PWROK

CLK_PCIE_PEG_REQ#

Q7601 PJV1702-R1-0000-GP (GP)
084.01702.0031
DIS

1D8V_AON_S0

R7601 10KR2J-3-GP DIS

VGA_RST#

GFX_CLKREQ_dGPU_N

GFX_CLK_CPU_P
GFX_CLK_CPU_N

GFX_PCIE_RX_P0 / GFX_PCIE_RX_N0 — C7601 1 / C7602 1 SCD22U10V2KX-2-GP DIS — GFX_PCIE_RX_CON_P0 / GFX_PCIE_RX_CON_N0
GFX_PCIE_TX_CON_P0 / GFX_PCIE_TX_CON_N0
GFX_PCIE_RX_P1 / GFX_PCIE_RX_N1 — C7603 1 / C7604 1 SCD22U10V2KX-2-GP DIS — GFX_PCIE_RX_CON_P1 / GFX_PCIE_RX_CON_N1
GFX_PCIE_TX_CON_P1 / GFX_PCIE_TX_CON_N1
GFX_PCIE_RX_P2 / GFX_PCIE_RX_N2 — C7605 1 / C7606 1 SCD22U10V2KX-2-GP DIS — GFX_PCIE_RX_CON_P2 / GFX_PCIE_RX_CON_N2
GFX_PCIE_TX_CON_P2 / GFX_PCIE_TX_CON_N2
GFX_PCIE_RX_P3 / GFX_PCIE_RX_N3 — C7607 1 / C7608 1 SCD22U10V2KX-2-GP DIS — GFX_PCIE_RX_CON_P3 / GFX_PCIE_RX_CON_N3
GFX_PCIE_TX_CON_P3 / GFX_PCIE_TX_CON_N3
GFX_PCIE_RX_P4 / GFX_PCIE_RX_N4 — C7609 1 / C7610 1 SCD22U10V2KX-2-GP DIS — GFX_PCIE_RX_CON_P4 / GFX_PCIE_RX_CON_N4
GFX_PCIE_TX_CON_P4 / GFX_PCIE_TX_CON_N4
GFX_PCIE_RX_P5 / GFX_PCIE_RX_N5 — C7611 1 / C7612 1 SCD22U10V2KX-2-GP DIS — GFX_PCIE_RX_CON_P5 / GFX_PCIE_RX_CON_N5
GFX_PCIE_TX_CON_P5 / GFX_PCIE_TX_CON_N5
GFX_PCIE_RX_P6 / GFX_PCIE_RX_N6 — C7613 1 / C7614 1 SCD22U10V2KX-2-GP DIS — GFX_PCIE_RX_CON_P6 / GFX_PCIE_RX_CON_N6
GFX_PCIE_TX_CON_P6 / GFX_PCIE_TX_CON_N6
GFX_PCIE_RX_P7 / GFX_PCIE_RX_N7 — C7615 1 / C7616 1 SCD22U10V2KX-2-GP DIS — GFX_PCIE_RX_CON_P7 / GFX_PCIE_RX_CON_N7
GFX_PCIE_TX_CON_P7 / GFX_PCIE_TX_CON_N7

GPU1A 1 OF 24
1/24 PCI_EXPRESS

BR31	PEX_WAKE#		
BT30	PEX_RST#		
BP31	PEX_CLKREQ#		
BJ30	PEX_REFCLK		
BK30	PEX_REFCLK#		
BL31	PEX_TX0	BJ32	PEX_RX0
BM31	PEX_TX0#	BK32	PEX_RX0#
BR32	PEX_TX1	BJ34	PEX_RX1
BT32	PEX_TX1#	BK34	PEX_RX1#
BP33	PEX_TX2	BL33	PEX_RX2
BR33	PEX_TX2#	BM33	PEX_RX2#
BR34	PEX_TX3	BJ36	PEX_RX3
BT34	PEX_TX3#	BK36	PEX_RX3#
BP35	PEX_TX4	BL35	PEX_RX4
BR35	PEX_TX4#	BM35	PEX_RX4#
BR36	PEX_TX5	BJ38	PEX_RX5
BT36	PEX_TX5#	BK38	PEX_RX5#
BP37	PEX_TX6	BL37	PEX_RX6
BR37	PEX_TX6#	BM37	PEX_RX6#
BR38	PEX_TX7	BJ40	PEX_RX7
BT38	PEX_TX7#	BK40	PEX_RX7#
BL39	PEX_TX8	BP41	PEX_RX8
BM39	PEX_TX8#	BR41	PEX_RX8#
BR40	PEX_TX9	BL41	PEX_RX9
BT40	PEX_TX9#	BM41	PEX_RX9#
BJ40	PEX_TX10	BR42	PEX_RX10
BK40	PEX_TX10#	BT42	PEX_RX10#
BP41	PEX_TX11	BJ42	PEX_RX11
BR41	PEX_TX11#	BK42	PEX_RX11#
BL41	PEX_TX12	BP43	PEX_RX12
BM41	PEX_TX12#	BR43	PEX_RX12#
BR42	PEX_TX13	BL43	PEX_RX13
BT42	PEX_TX13#	BM43	PEX_RX13#
BJ42	PEX_TX14	BR44	PEX_RX14
BK42	PEX_TX14#	BT44	PEX_RX14#
BP43	PEX_TX15	BJ44	PEX_RX15
BR43	PEX_TX15#	BK44	PEX_RX15#

NG-GN20-E3-MAX-Q-GP
071.0GN20.0A0U
DIS

1V_VGA_S0

PEX_DVDD_1	BF32
PEX_DVDD_2	BF34
PEX_DVDD_3	BF35
PEX_DVDD_4	BF37
PEX_DVDD_5	BG32
PEX_DVDD_6	BG34
PEX_DVDD_7	BG35
PEX_DVDD_8	BG37
PEX_DVDD_9	BH32
PEX_DVDD_10	BH34
PEX_DVDD_11	BH35
PEX_DVDD_12	BH37
PEX_CVDD_1	BF31
PEX_CVDD_2	BG31
PEX_CVDD_3	BH31

Place under GPU: 6x0201 1uF X6S (C7638 C7643 C7646 C7649 C7651 C7637) DIS
Place near GPU: 3x0603 10uF X6S (C7656 C7658 C7660) DIS; 2x0603 22uF X6S (C7662 C7665 C7623 C7624) DIS
2x0603 4.7uF X6S (C7621 C7622 C7648 C7652) DIS

1D8V_AON_S0

PEX_HVDD_1	BF38
PEX_HVDD_2	BF40
PEX_HVDD_3	BF41
PEX_HVDD_4	BG38
PEX_HVDD_5	BG40
PEX_HVDD_6	BG41
PEX_HVDD_7	BG43
PEX_HVDD_8	BG44
PEX_HVDD_9	BG38
PEX_HVDD_10	BH40
PEX_HVDD_11	BH41
PEX_HVDD_12	BH43
PEX_HVDD_13	BH44
PEX_PLL_HVDD	BF43

Place near balls: 9x0201 1uF X6S (C7636 C7641 C7666 C7667 C7668 C7635 C7640 C7644 C7647) DIS
Place near GPU: 3x0603 10uF X6S (C7657 C7655 C7661) DIS; 2x0603 22uF X6S (C7663 C7664 C7625 C7626) DIS
2x0603 4.7uF X6S (C7619 C7620 C7669 C7670) DIS

1D8V_AON_S0

Place under GPU: 1x0201 1uF X6S (C7617 C7618 C7633) DIS

DA-09940-004_v01_STD_PCB_REF_SCH P.3

PEX_PLL_HVDD — BF43 — PEX_PLL_HVDD_1V — L102 — C317 1UF 4V ±10% X5R 0402 — GND

PEX_CVDD_SENSE — BK46

PEX_TERMP — BT50

R7602 1 DIS 2 2K49R1F-GP

R7602 Close to GPU

DG-09845-001_v01 P.128

PEX_TERMP is used for internal calibration; pull down this signal with a 2.49 k 1% resistor.

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Title: 076_GPU (PEG 1/5_GN20E3)

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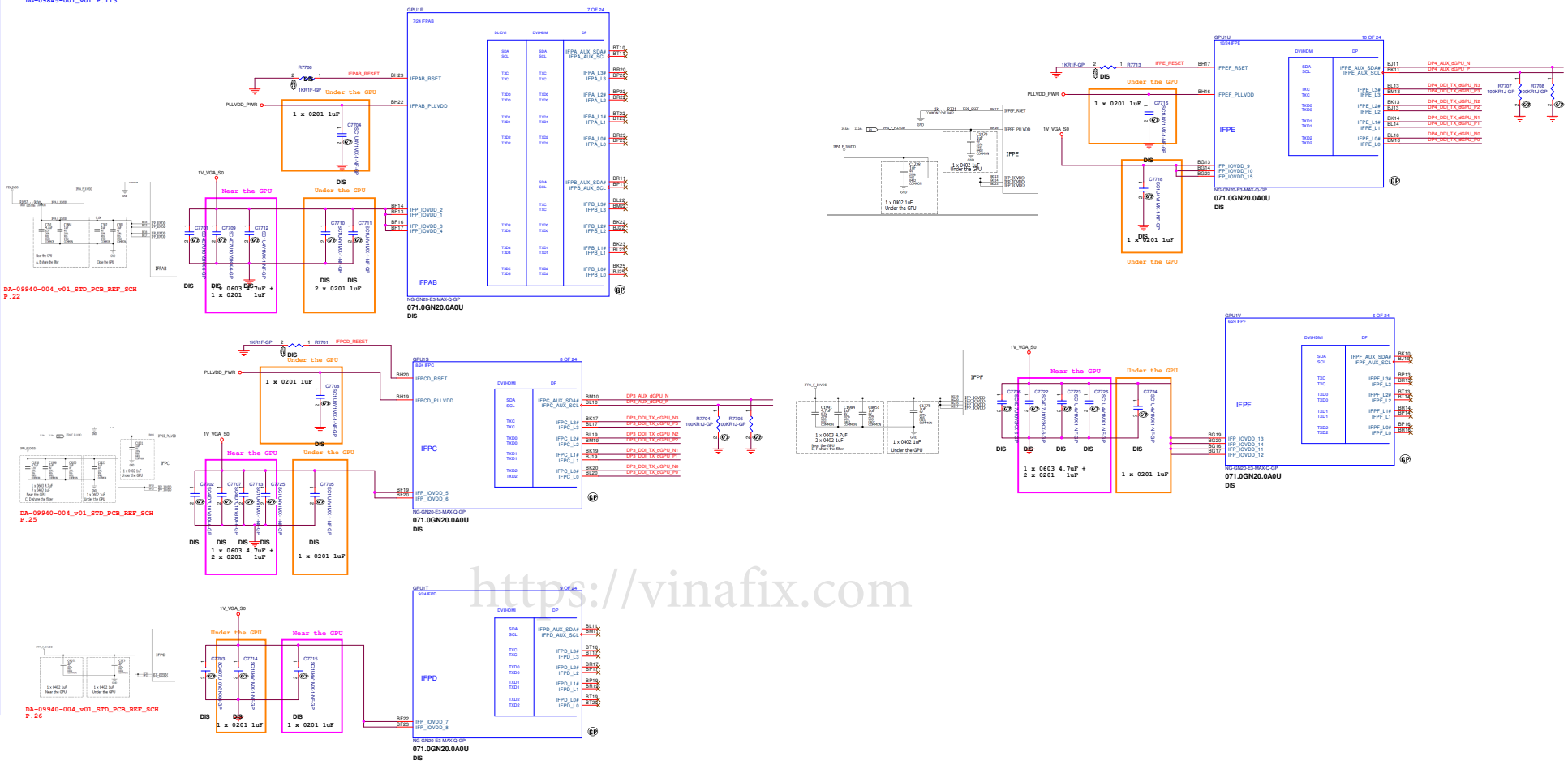
Main Func = dGPU

For DisplayPort and DVI support, all dual-link IFP macros (IFPAB, IFPCD, IFPEF) require the IFPxx_RSET pin to be pulled down via a 1 kΩ (1% precision) pull-down resistor to ground. Each IFPxx_RSET pin should be configured with 1 kΩ pull down resistor.

DG-09845-001_v01 P.113



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DG-09845-001_v01 P.112

Table 7.1 Display Link Summary (GB5-256 packages)

Digital Display Link	Dual-Link DVI	HDMI	eDP	DisplayPort
IFPA (Link A)	✓(Dual Link with IFPB)			✓
IFPB (Link B)	✓(Dual Link with IFPA)			✓
IFPC (Link C)		✓		✓
IFPD (Link D)			✓	
IFPE (Link E)		✓		✓
IFPE (Link F)				✓

Table 7.2 Display Link Power Rail Applicability

Display Link Rail	DISPLAY LINKS THAT RECEIVE POWER FROM THIS RAIL					
	Link A	Link B	Link C	Link D	Link E	Link F
IFP_IOVDD	✓	✓	✓	✓	✓	✓
IFPAB_PLLVDD	✓	✓				
IFPCD_PLLVDD			✓	✓		
IFPEF_PLLVDD					✓	✓

GN20E_GB5-256_MBD_AE_Checklist_v04, Display

1, If an IFP link is unused,in general it should be left unconnected.This includes Main and Aux links.
2, IFPxy_REST can be left unconnected and IFPxy_PLLVDD(xy=AB,CD,EF) should be 10K PD to GND if neither of IFPx/IFPy is in use.
3, IFP_IOVDD rail can be unconnected if no IFP link is used.
4, If any IFP is used,all IFP_IOVDD balls must be connected to power rail.

DG-09845-001_v01 P.46

Rail (GPU Ball Name)	Balls	Voltage	Filtering under GPU	Filtering near GPU
CORE_PLL_AVDD GPCADC_AVDD SP_PLLVDD VID_PLLVDD IFPAB_PLLVDD IFPCD_PLLVDD IFPEF_PLLVDD	1 1 1 1 1 1 1	1.8V	6 x 1uF (0402 X6S) (1 per ball)	1 x 30Ω bead (0603 max ESR 10 mΩ) 1 x 22uF (0805) 1 x 4.7uF (0603 X6S)
IFP_IOVDD_x (x=1-15)	15	0.95V	5 x 1uF (0402 X6S)	3 x 4.7uF (0603 X6S) 5 x 1uF (0402 X6S)

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077_GPU (DIGITAL 2/5)

Size: A1 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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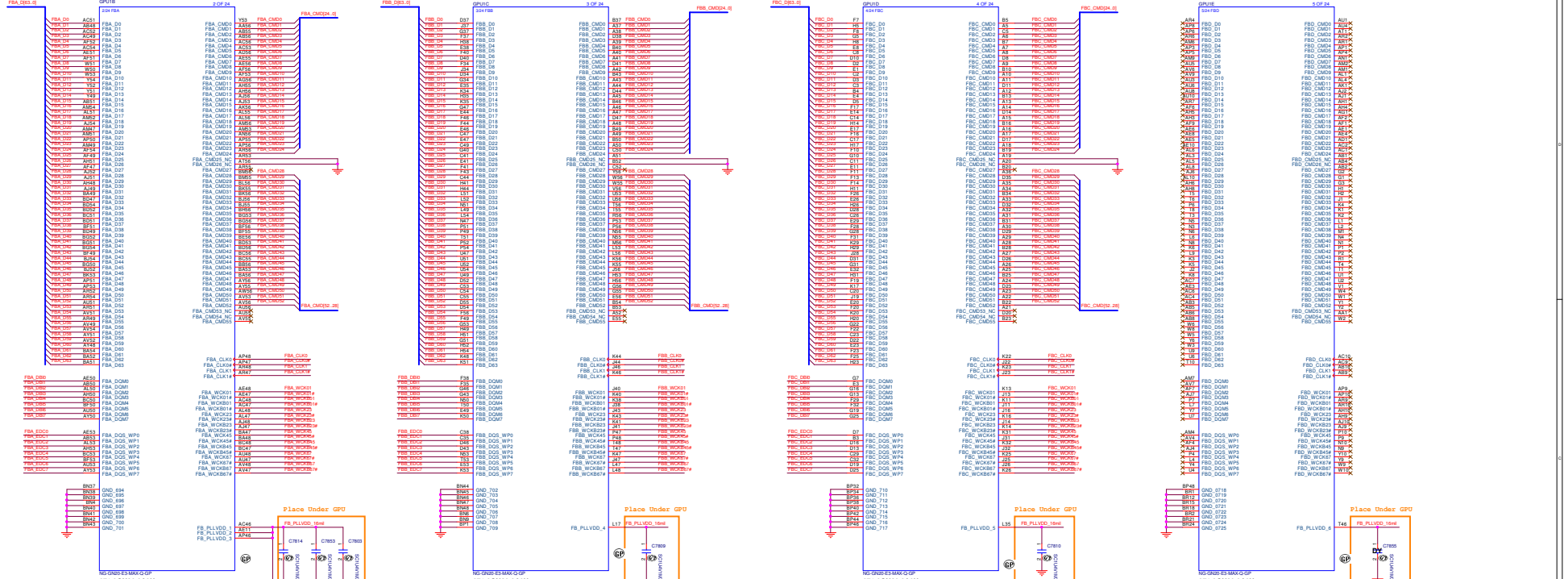
Group A

Group B

Group C



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GN20E_GB5-256_MBD_AE_Checklist_v04, GDDR6

1. Should be left floating.
2. For example, a design using 192 bits of memory with a GB5-256 package would have to leave the unused 64 data-bits and associated command/address pins floating.
1. FBx_PLL_AVDD should be connected per power and decoupling requirements.
1. FBx_CMD25..FBx_CMD 28..FBx_CMD 53..FBx_CMD 54 can be either connect to GND or NC. GND is prefer

DG-09845-001_v02 P.46

Rail (GPU Ball Name)	Balls	Voltage	Filtering under GPU	Filtering near GPU
FBVDDQ (GPU side)[1]	58	1.20V 1.25V 1.35V	24 x 10uF (0402 or 0201W X6S) 8 x 10uF (0603 X6S)	9 x 10uF (0603 X6S) 9 x 22uF (0603 X6S)
FB_PLLVDD_x (x=1~6)	6	1.8V	4 x 1uF (0402 or 0201W X6S) (1 per ball)	1 x 300 bead (0603 max ESR 10 mΩ) 1 x 22uF (0805) 1 x 4.7uF (0603 X6S)

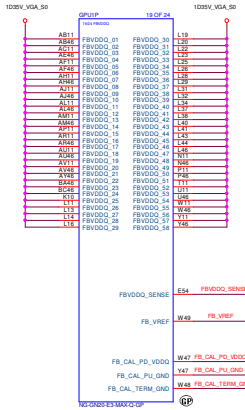
Place Under GPU

24 x 0201 1uF (X6S) +
8 x 0603 10uF (X6S)

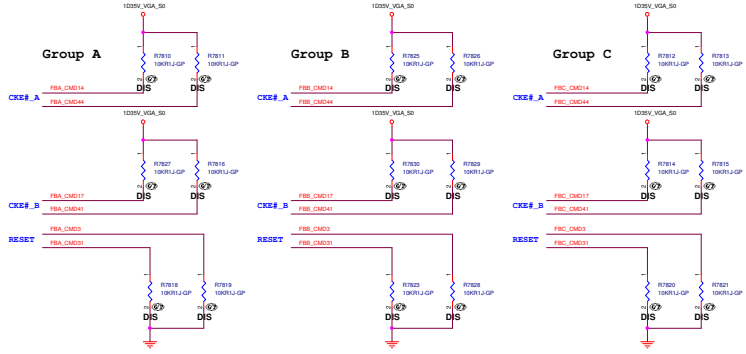
Place close to GPU

5 x 0603 10uF (X6S)+
9 x 0603 22uF (X6S)

MEM_VDD_CTL: High -> FBVDD=1.35V
MEM_VDD_CTL: Low -> FBVDD=1.25V



FBCLK Termination place on VRAM side

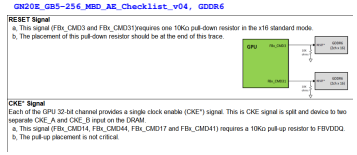


GN20E_GB5-256_MBD_AE_Checklist_v04, GDDR6

DG-09845-001_v02 P.88

6.2.2.13 Memory Voltage Reference (VREF)

The GPUs have an integrated VREF reference, therefore do not require an external VREF reference circuit. The GPU's FB_VREF pin should be tied to GND via a 2.49 kΩ 1% resistor in parallel with a 3.9 pF capacitor.



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078_GPU (VRAM 3/5)

Size: Document Number: Cyborg_TGL-H RTX — Rev: X01

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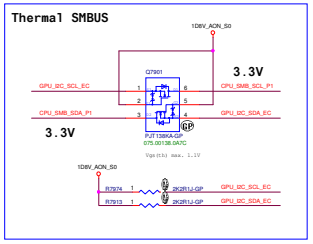
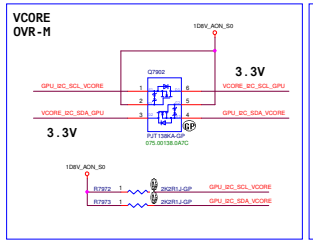
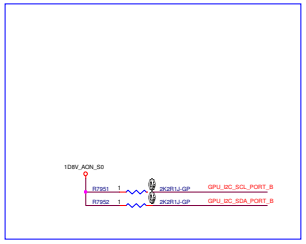
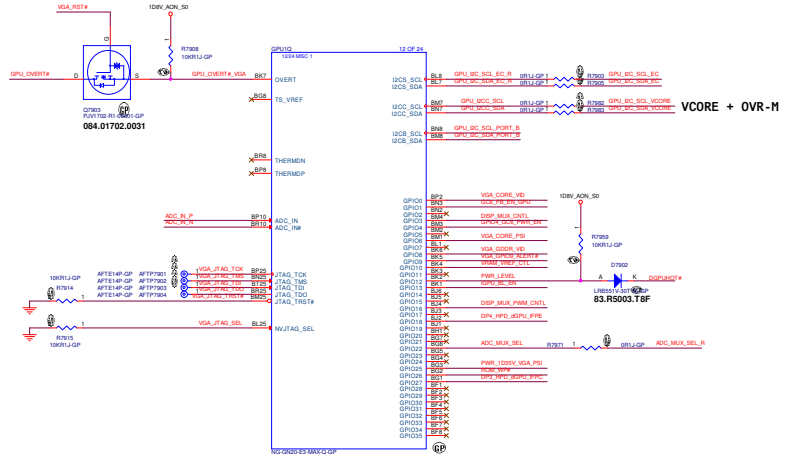
Thermal SMBUS



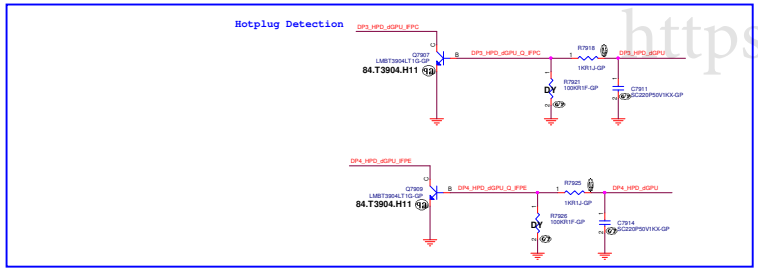
VCORE OVR-M



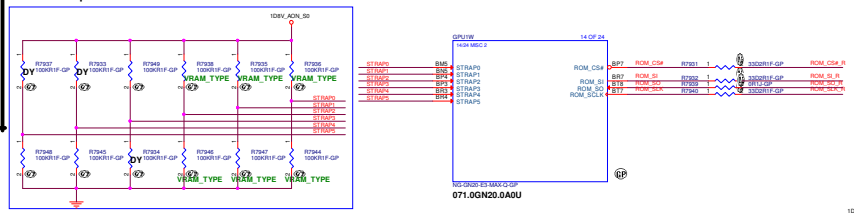


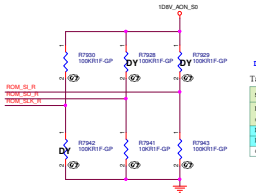


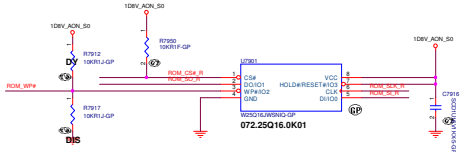
Hotplug Detection



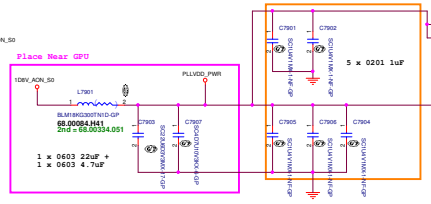
Strap Pin

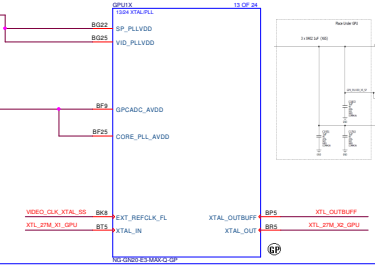




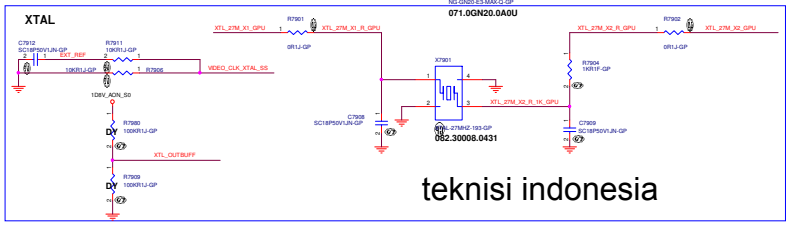


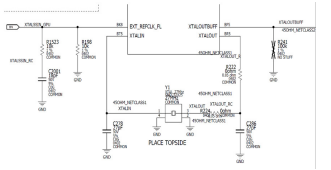
Place Under GPU

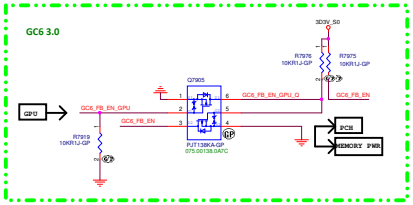


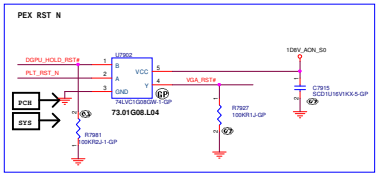


XTAL









DG-09845-001_v02 P.168

Table 13.2 I2C Availability by GPU Package

GPU Package(s)	Signal Name	Type	Application	Associated Display Link	Voltage Tolerance
685-2G4 0B58-178	Bus 0 SCL I2C0_SCL DC0_SCL	Bus Master	Assigned to DP port for Aux (like) AUX/I2C over AUX, Panel I2C interface	N/A	3.3V
	Bus 0 SDA I2C0_SDA DC0_SDA	Bus Master	NVIDIA GPU use only including DVI-I# SDVO, DVI#	N/A	3.3V
	Bus 0 S DC0_SDA	Slave	SMBus/ internal thermal sensor	N/A	3.3V

GN20E_GB5-256_MBD_AE_Checklist_v04, GPIO

GPIO Descriptions for Packages:GB5-256

Balls P5 Name	GPIO Name	I/O	Functional Description	I/O Termination
GPIO00	MVVDD_PWM_VID	O	PWM Output to control NVVDD	No Pull Up or Down
GPIO01	GC6/GC6_FB_EN	I/O	FB Enable for GC6	10KΩ Pull Down
GPIO02	UNUSED	I/O		
GPIO03	DISP_MUX_CNTL	O	Display MUX control signal that provides the ability to switch the AUX and main link between integrated GPU (iGPU) and discrete GPU (dGPU) sources. Init settings should be 0 (indicating integrated GPU).	10KΩ Pull Down
GPIO04	MVVDD_EN (Split Rail) MVVDD_EN (Merged Rail)	O	GPU power sequencing for GC6	10KΩ Pull Up to 1V8
GPIO05	FRAME_LOCK*	O	Frame lock	10KΩ Pull Up to 1V8
GPIO06	NVVDD_PSI*	O	The PSI signal should follow E3908 and refer to OVR controller spec	Stuff 10K resistor on R1 and R2 depending on PSI topology
GPIO07	LCD_BL_PWM	O	LCD Panel Backlight PWM	100KΩ Pull Down
GPIO08	MEM_VDD_CTL	O	1. Memory voltage control 2. PWM VID support (with MEM_VDD_CTL) for FBVDD regulator is inadditory. Partners must use OVR regulator as listed in the power RVL(BVL-69003). Please keep BOM option to control FBVDD voltage with VHF.	PU/PD to set the FBVDD/Q power-on voltage
GPIO09	THERM_ALERT*	I/O	Active Low Thermal Alert	10KΩ Pull Up to 1V8
GPIO10	GPU_I2C_SCL_CTL	I/O	GPU I2C Clock Control	10KΩ Pull Down
GPIO11	LCD_VDD	O	Panel power enable	10KΩ Pull Down
GPIO12	PWR_LEVEL	I	AC power detect for power supply overdrive input	10KΩ Pull Up to 1V8
GPIO13	AGPU_BL_EN	O	PWM Signal indicating when the IGPU has enabled the BL. This can be interpreted as IGPU blanked displaying to display in a DGPU to IGPU switch sequence.	10KΩ Pull Up to 1V8
GPIO14	HPD_IFPA*	I	Hot Plug Detect for IFPA	10KΩ Pull Up to 1V8
GPIO15	HPD_IFPB* or LCD_BIAS or DONGLE_DET*	I	Hot Plug Detect for IFPB	10KΩ Pull Up to 1V8
GPIO16	DISP_MUX_PWM_CNTL	O	LCD/O/Above indicating the PWM between the IGPU and DGPU. Init settings should be 0 (indicating IGPU)	10KΩ Pull Down
GPIO17	HPD_IFPD*	I	Hot Plug Detect for IFPD	10KΩ Pull Up to 1V8
GPIO18	HPD_IFPE*	I	Hot Plug Detect for IFPE	10KΩ Pull Up to 1V8
GPIO19	UNUSED	O		
GPIO20	UNUSED	IO		
GPIO21	LCD_BLEN	O	LCD Panel Backlight enable	100KΩ Pull Down
GPIO22	ADC_MUX_SEL	O	OVR-M Mux input Select	2.2K pull up to 1V8
GPIO23	UNUSED	O		
GPIO24	HPD_IFPF*	I	Hot Plug Detect for IFPF	10KΩ Pull Up to 1V8
GPIO25	FBVDD_PSI*	O	The PSI signal should follow E3908 and refer to OVR controller spec	Stuff 10K resistor on R1 and R2 depending on PSI topology
GPIO26	ROM_WP*	O	connect to WP (Write Protect) pin of the GPU EEPROM	10KΩ Pull-Down
GPIO27	HPD_IFPC*	I	Hot Plug Detect for IFPC	10KΩ Pull-Up to 1V8
GPIO28	MVVDD_PWM_VID	O	PWM Output to control NVVDD#5	No Pull Up or Down
GPIO29	NVVDD_EN (Split Rail) NC (Merged Rail)	O	NVVDD enable	
GPIO30	MSVDD_PSI*		Phase Shedding	NC
GPIO31	UNUSED			
GPIO32	UNUSED			Will update on next HW design guide
GPIO33	UNUSED			Will update on next HW design guide

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Table 9.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function DISABLED
L	L	H	FS_OVERT* function ENABLED (default)
all other configurations			(Invalid, do not configure)

DG-09845-001_v02 P.139

Table 9.3 RAMCFG

Strap Pins see Note			RAMCFG Strap Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x00000)
L	L	H	1 (0x00001)
L	H	L	2 (0x00002)

RVL-09964-001_v01 P.7

Table 3. GN20-E3 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	32Mx256Mx16	1.35V	Samsung	K4ZAB325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate
		1.25V	Hynix	H5AC8G1GAAR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
		1.2V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	YWD	Full	Production candidate

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Table 9.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	M	L	1	0	0	0
L	M	H	1	0	0	1
L	H	M	1	0	1	0
L	H	L	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

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Title: 079_GPU (GPIO_STRAP 4/5)

Size: A1 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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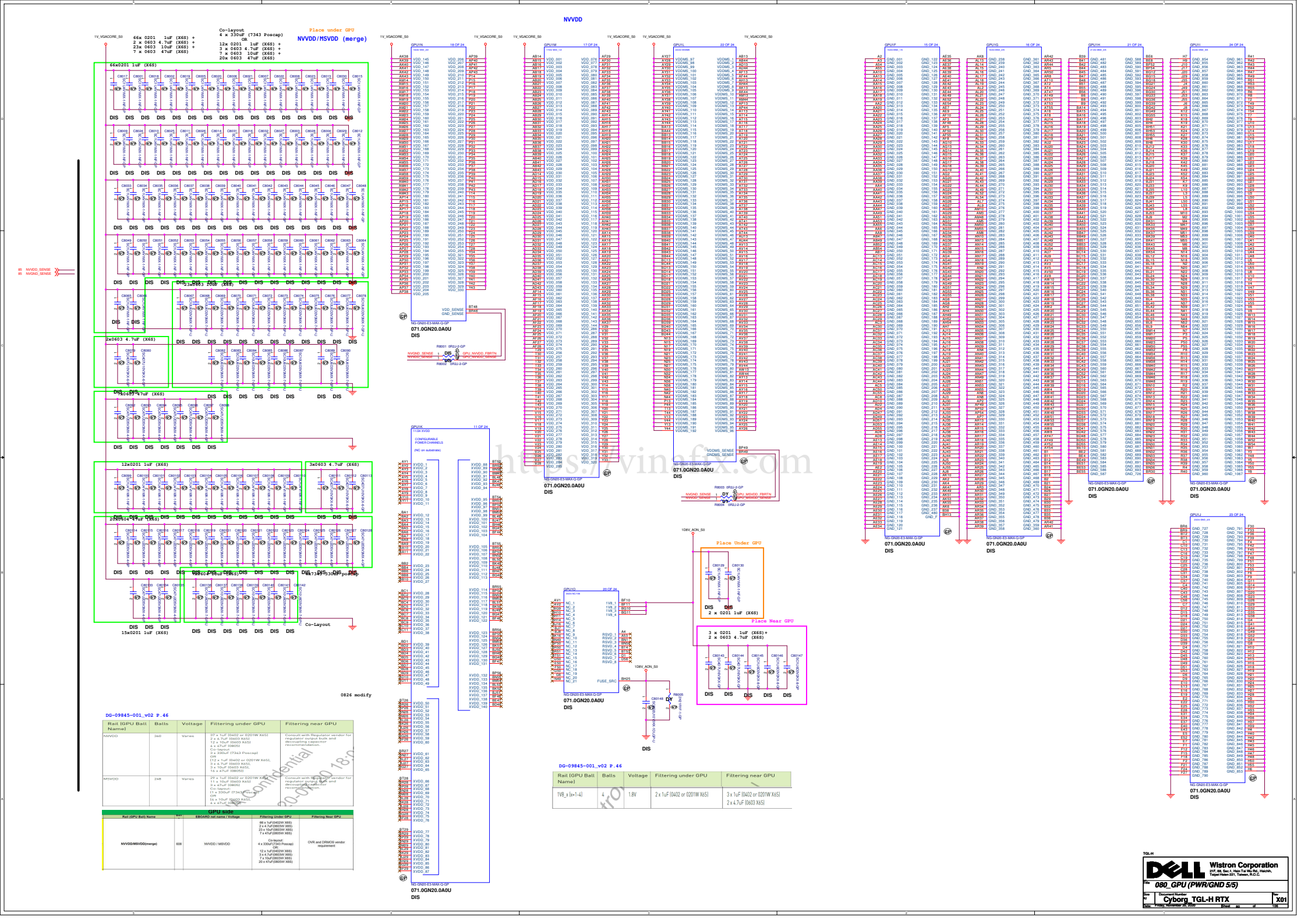
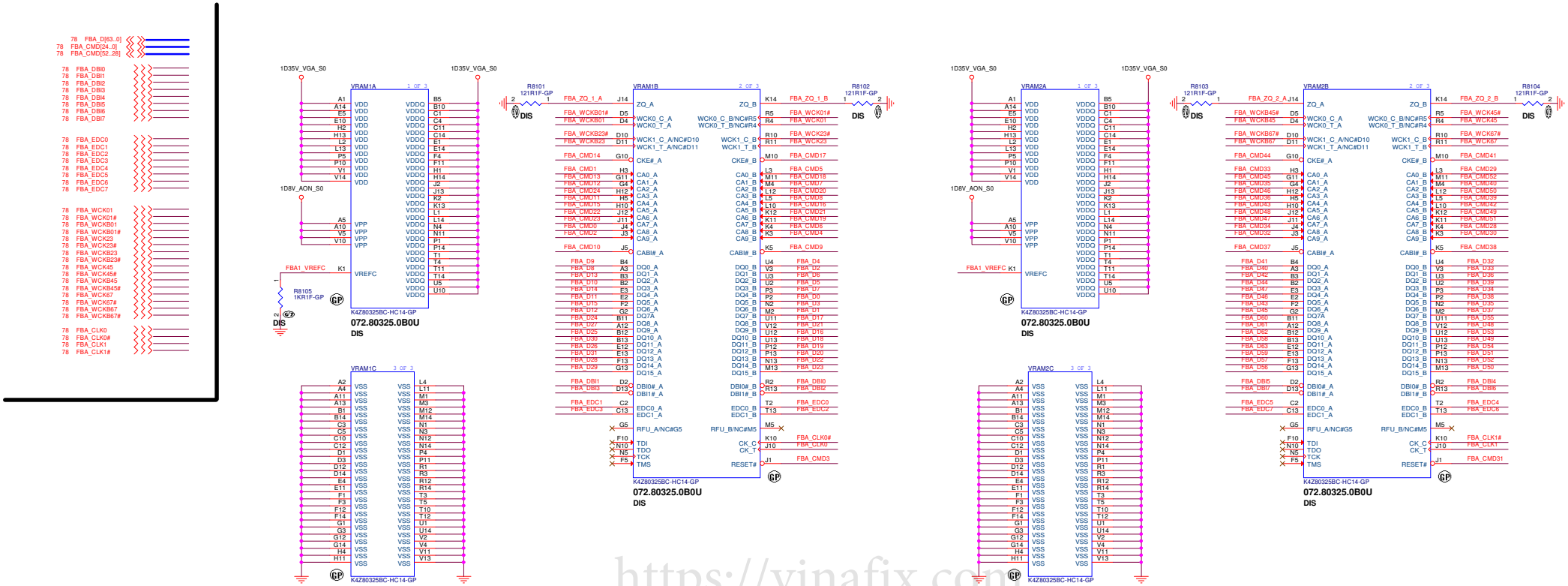

NVVDD
Place under GPU
NVVDD/MSVDD (merge)
Co-layout
4 x 330uF (7343 Poscap)
OR
12x 0201 1uF (X6S) +
3 x 0603 4.7uF (X6S) +
7 x 0603 10uF (X6S) +
20x 0603 47uF (X6S)
66x0201 1uF (X6S)
23x0603 10uF (X6S)
2x0603 4.7uF (X6S)
10x0603 47uF (X6S)
12x0201 1uF (X6S)
3x0603 4.7uF (X6S)
20x0603 47uF (X6S)
15x0201 1uF (X6S)
Co-Layout
0826 modify
DG-09845-001_v02 P.46
Rail (GPU Ball Name)
Balls
Voltage
Filtering under GPU
Filtering near GPU
NVVDD
360
Varies
37 x 1uF (0402 or 0201W X6S)
2 x 4.7uF (0603 X6S)
12 x 10uF (0603 X6S)
(or 10805)
Co-layout:
3 x 330uF (7343 Poscap)
OR
[12 x 1uF (0402 or 0201W X6S),
3 x 4.7uF (0603 X6S),
3 x 10uF (0603 X6S),
16 x 47uF (0805S)]
Consult with Regulator vendor for regulator output bulk and decoupling capacitor recommendation.
MSVDD
248
Varies
29 x 1uF (0402 or 0201W X6S)
11 x 10uF (0603 X6S)
3 x 47uF (0805)
Co-layout:
[1 x 330uF (7343 Poscap)
OR
16 x 10uF (0603 X6S),
4 x 47uF (0805)]
Consult with Regulator vendor for regulator output bulk and decoupling capacitor recommendation.
GPU side
Rail (GPU Ball) Name
Balls
EBOARD net name / Voltage
Filtering Under GPU
Filtering Near GPU
NVVDD/MSVDD(merge)
608
NVVDD / MSVDD
66 x 1uF(0402W X6S)
2 x 4.7uF(0603W X6S)
23 x 10uF(0603W X6S)
7 x 47uF(0805W X6S)
Co-layout:
4 x 330uF (7343 Poscap)
OR
[12 x 1uF(0402W X6S)
3 x 4.7uF(0603W X6S)
7 x 10uF(0603W X6S)
20 x 47uF(0805W X6S)]
OVR and DRMOS vendor requirement
DG-09845-001_v02 P.46
Rail (GPU Ball Name)
Balls
Voltage
Filtering under GPU
Filtering near GPU
1V8_x (x=1-4)
4
1.8V
2 x 1uF (0402 or 0201W X6S)
3 x 1uF (0402 or 0201W X6S)
2 x 4.7uF (0603 X6S)
Place Under GPU
Place Near GPU
3 x 0201 1uF (X6S) +
2 x 0603 4.7uF (X6S)
071.0GN20.0A0U
DIS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
080_GPU (PWR/GND 5/5)
Cyborg_TGL-H RTX
X01
Friday, November 20, 2020
Sheet 80 of 106
TGL-H



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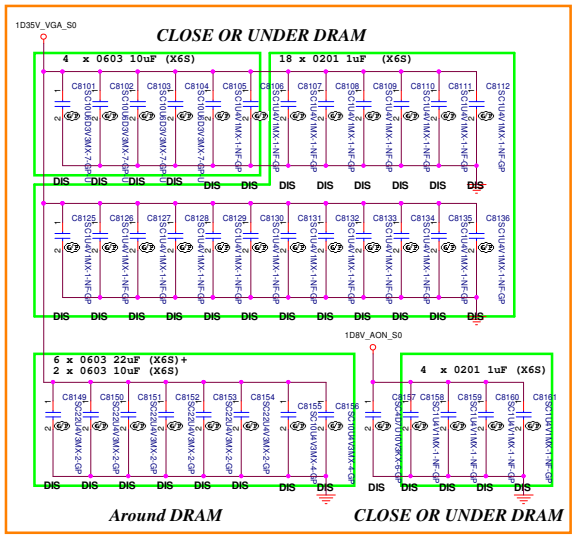
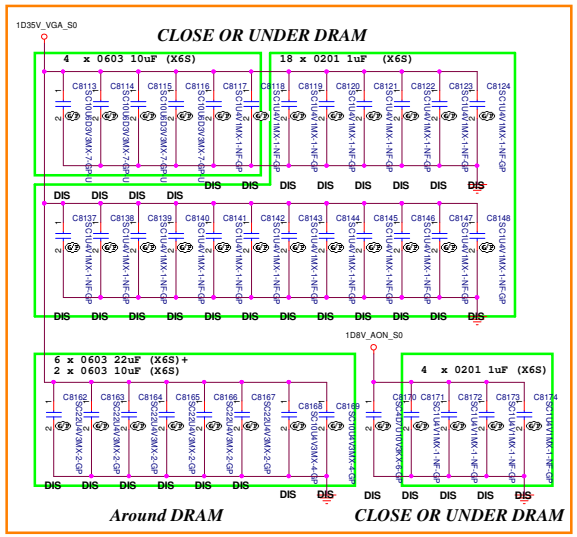
FOR VRAM1



FOR VRAM2

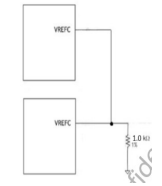


DG-09845-001_v02 P.89

6.2.2.14 GDDR6 DRAM VREFC

GDDR6 DRAMs include an integrated VREFC (VREF for CMD and ADDR). Figure 6.7 illustrates use of the integrated VREFC for x16 mode GDDR6 DRAMs. Refer to the reference schematics for final component values. If using the integrated VREFC, the VREFC pin should be tied to GND via a 1 kΩ 1% resistor.

Figure 6.6 Use of Integrated VREFC for ×16 Mode



Size	Value	Location	Quantity	Notes
0201/0402	1uF, X6S	Close or Under DRAM	18	Can use 0402 X6S or 0201 X6S
0603	10uF, X6S		4	
0603	10uF, X6S	Around DRAM	2	MLCC caps should be implemented first, and add POSCAP as optional
0603	22uF, X6S		6	
POSCAP	220uF/330uF , -55C to 105C	Under or around DRAM	1	Recommended for spare area (near or under DRAM) after fulfilling of all MLCC caps Especially for DRAMs from FBVDD Regulator output caps

Note: [1] Add 4x 1uF(0201/0402, X6S) for 1.8V VPP rail (Close or under memory).

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Title: 081_GPU (VRAM1,2 1/4)

Size: A2 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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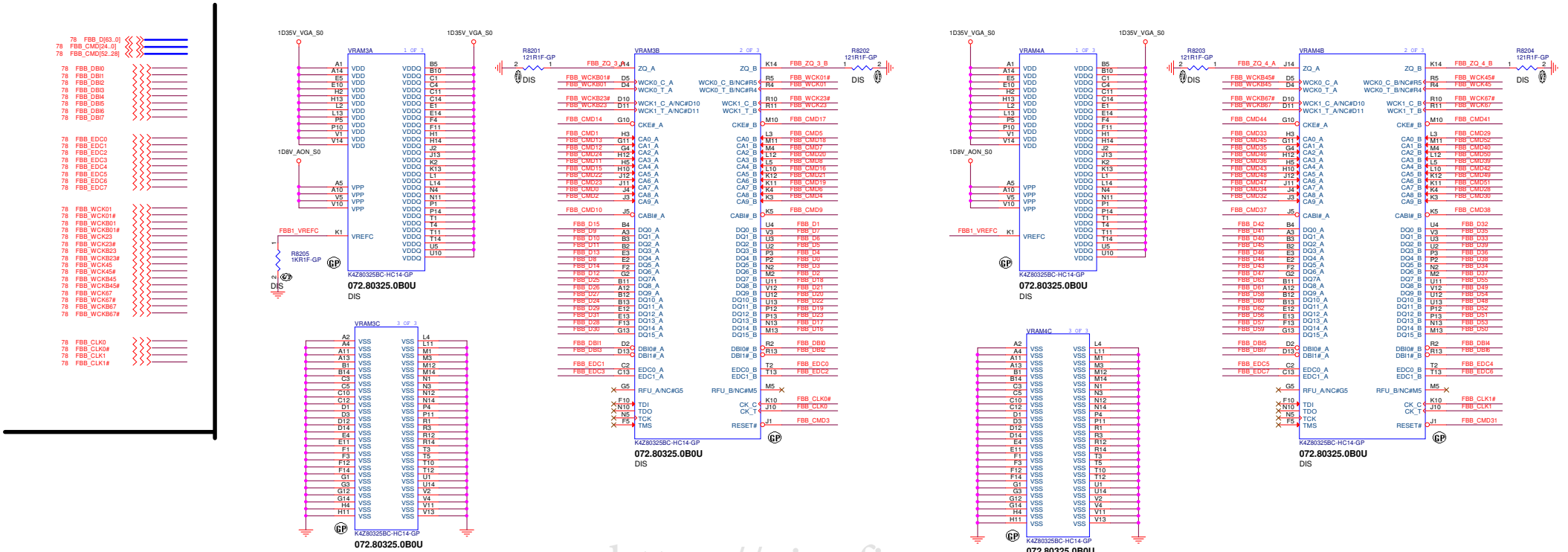

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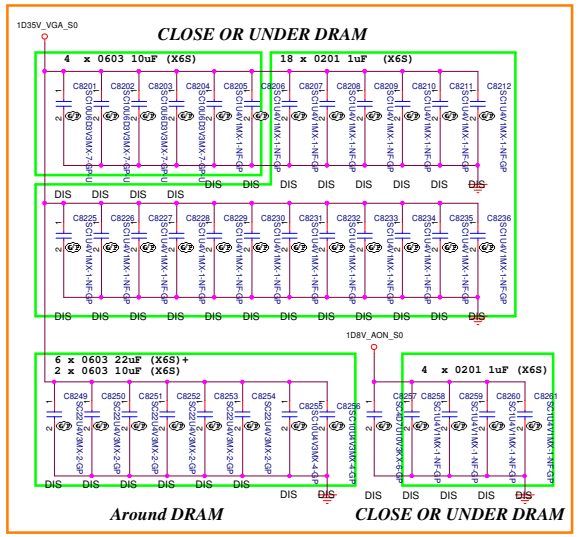
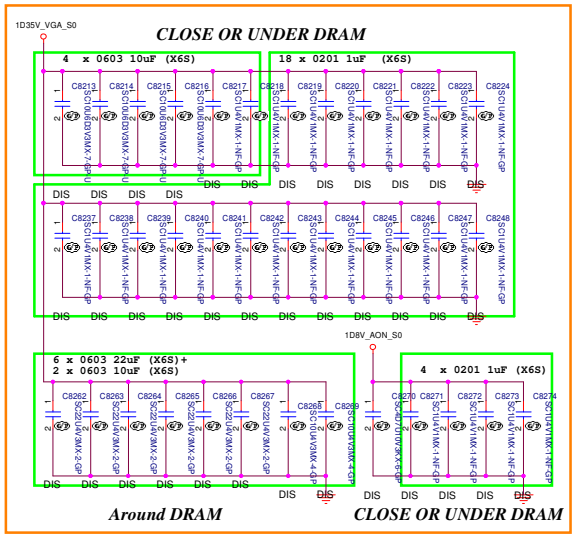
FOR VRAM3



FOR VRAM4



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Size	Value	Location	Quantity	Notes
0201/0402	1uF, X6S	Close or Under DRAM	18	Can use 0402-X6S or 0201 X6S
0603	10uF, X6S		4	
0603	10uF, X6S	Around DRAM	2	MLCC caps should be implemented first, and add POSCA as optional
0603	22uF, X6S		6	
POSCAP	220uF/330uF , -55C to 105C	Under or around DRAM	1	Recommended for spare area (near or under DRAM) after fulfilling of all MLCC caps Especially far DRAMs from FBVDD Regulator output caps

Note: [1] Add 4x 1uF(0201/0402, X6S) for 1.8V VPP rail (Close or under memory).

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Title: 082_GPU (VRAM3,4 2/4)

Size: A2 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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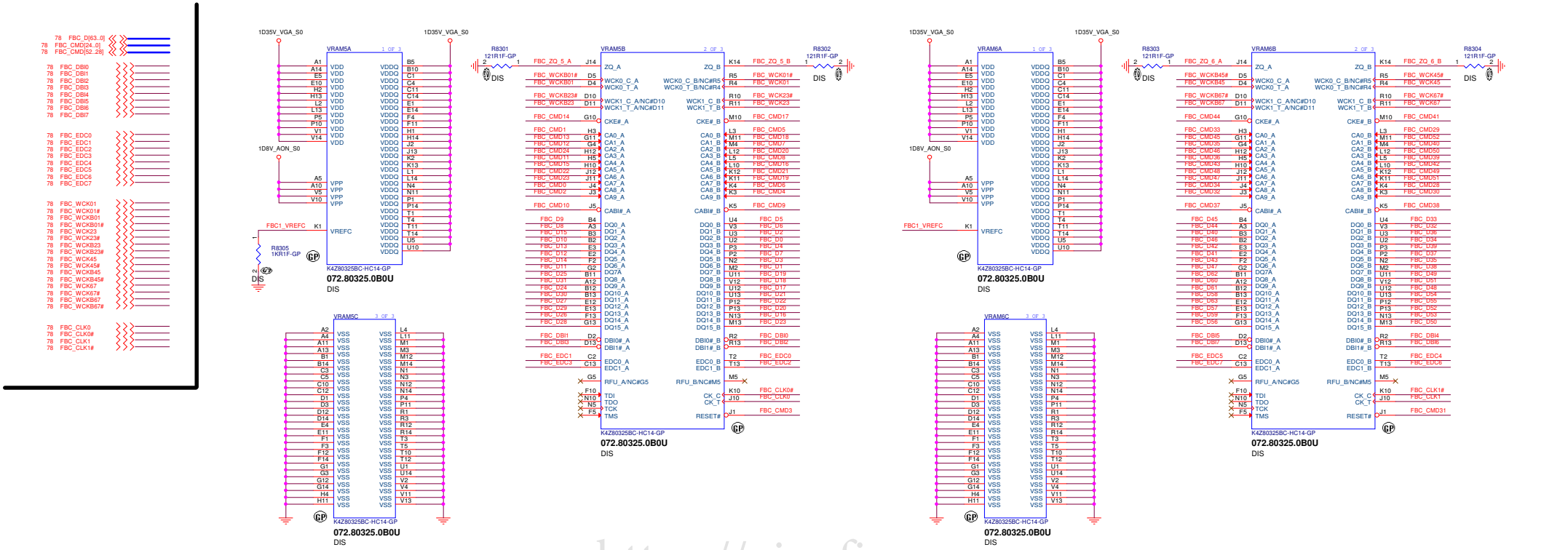

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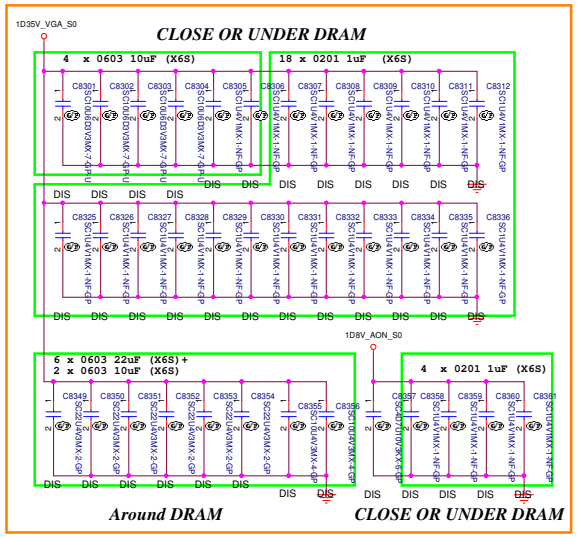
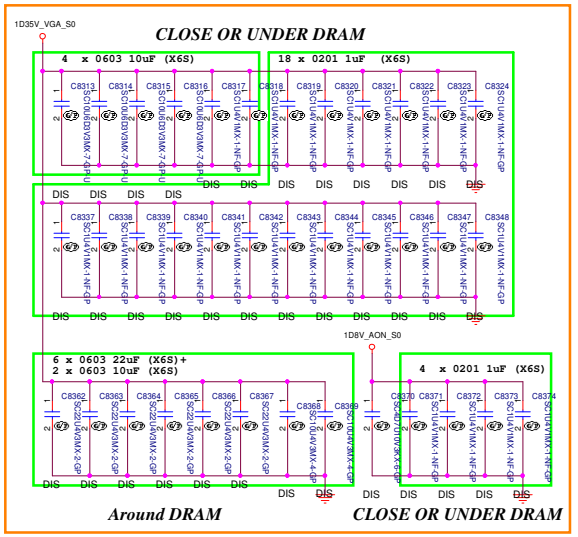
FOR VRAM5



FOR VRAM6



Size	Value	Location	Quantity	Notes
0201/0402	1uF, X6S	Close or Under DRAM	18	Can use 0402 X6S or 0201 X6S
0603	10uF, X6S		4	
0603	10uF, X6S	Around DRAM	2	MLCC caps should be implemented first, and add POSCAP as optional
0603	22uF, X6S		6	
POSCAP	220uF/330uF, -55C to 105C	Under or around DRAM	1	Recommended for spare area (near or under DRAM) after fulfilling of all MLCC caps Especially for DRAMs from FBVDD Regulator output caps

Note: [1] Add 4x 1uF(0201/0402, X6S) for 1.8V VPP rail (Close or under memory).

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Title: 083_GPU (VRAM5,6 3/4)

Size: A2 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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Title: 084_GPU (VRAM7,8 4/4)

Size: A3 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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MP2884A For VGA core

VGA : GN20-E3 MAXQ
EDP-Continuous : 65 A
EDP-Peak : 225 A

OFFPAGE

OVR (RSVD)

Need close to GPU

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification		
	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{OMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.499
C	nF	0.1

Table 7.9 PWM-VID Spec and Component Values

PWM-VID Specification		
		Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{OMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.499
C	nF	0.1

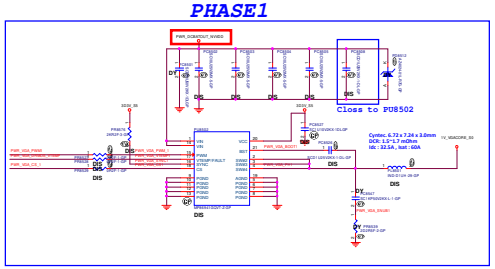
MP2884AGU-0916-GP
074.02B84.M009

	PR8590	PR8591	PR8592	PR8593	PHASE5	PHASE6
6 Phase	DY	DY	DY	DY	stuff	stuff
4 Phase	10kOhm	10kOhm	DY	DY	DY	DY
3 Phase	10kOhm	10kOhm	10kOhm	DY	DY	DY
2 Phase	10kOhm	10kOhm	10kOhm	10kOhm	DY	DY

ADDR Setting

GC6 3.0

PHASE1



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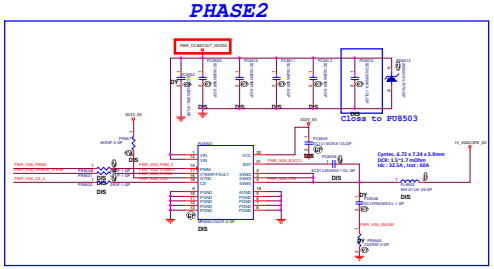

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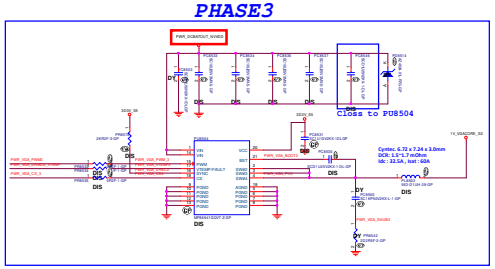

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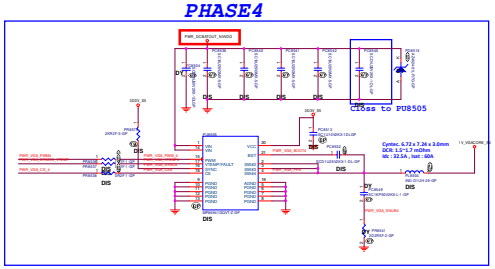
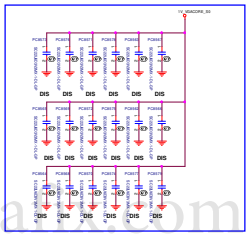
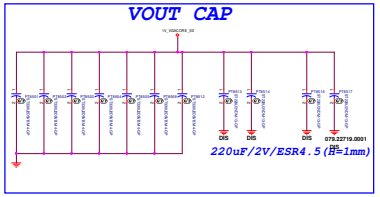


Vout MLCC



VOUT CAP



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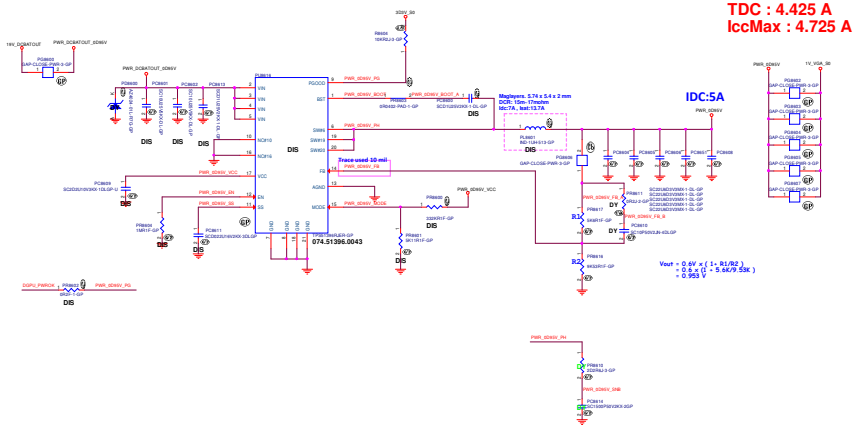
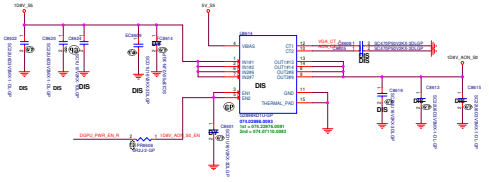
GPU VCORE POWER	
Project Name: Cyborg TGL-H RTX	X01

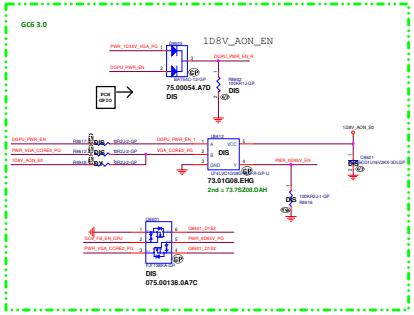
OFFPAGE

TPS51396 for 0D95V_VGA_S0



G2898 for 1D8V_AON_S0





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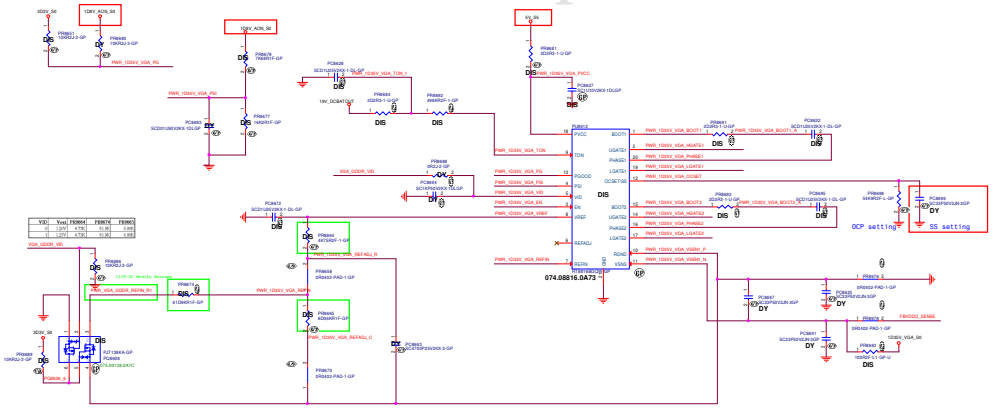
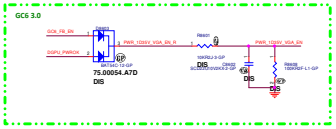
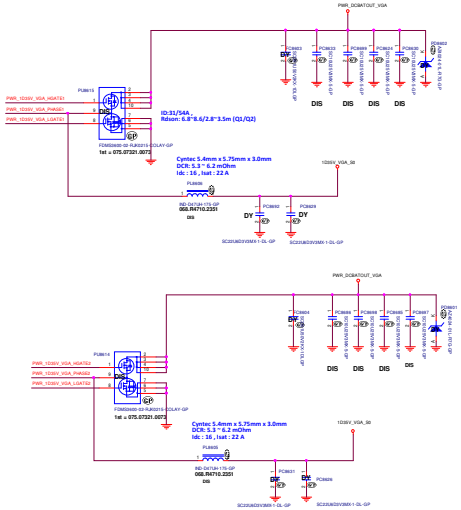


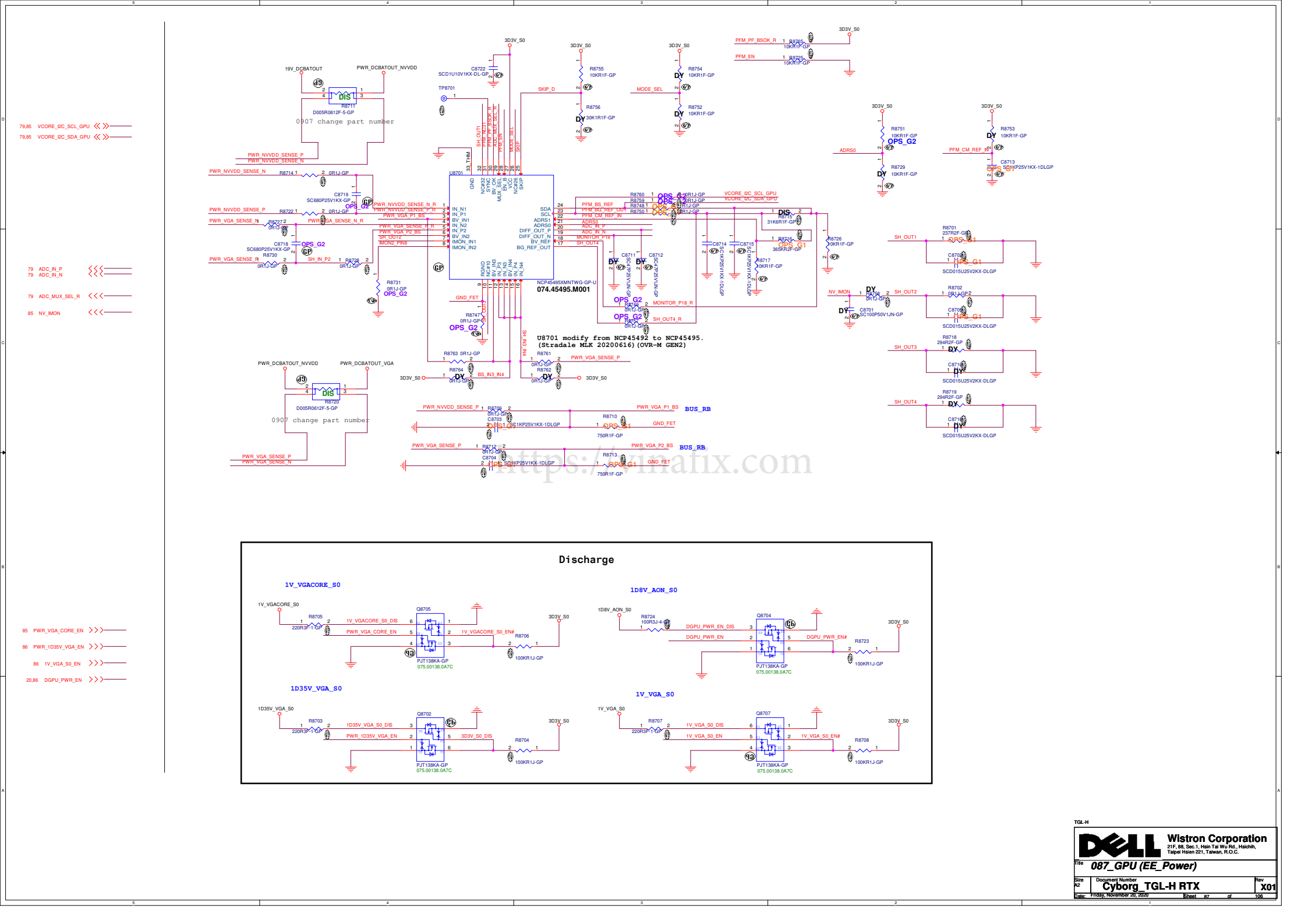
		PR8664(K)	PR8665(K)	PR8674(K)
GDDR6	1.25/1.2v	4.75	8.06	61.9
GDDR5	1.5/1.35	4.75	14.3	33

	PR8664	PR8665	PR8674
1.5V/1.35V	4.75K	14.3K	33K
1.2V Fb	4.75K	7.15K	6C
1.35V/1.25V	4.75K	10K	40.2K





Wistron Corporation	
GPU (Power_others)	
Cyborg_TGL-H RTX	X01



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Title: 087_GPU (EE_Power)

Size: A2 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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Title: *GPU (Discharge/Sequence)*

Size	Document Number	Rev
A3	Cyborg_TGL-H RTX	X01

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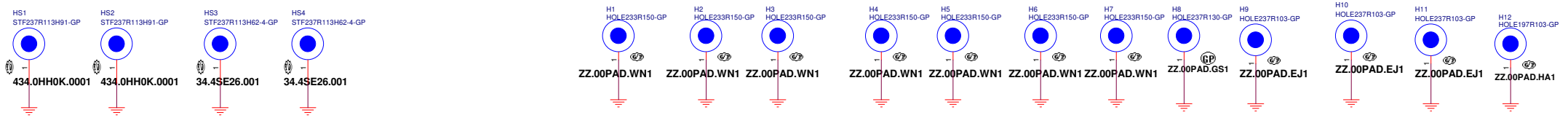
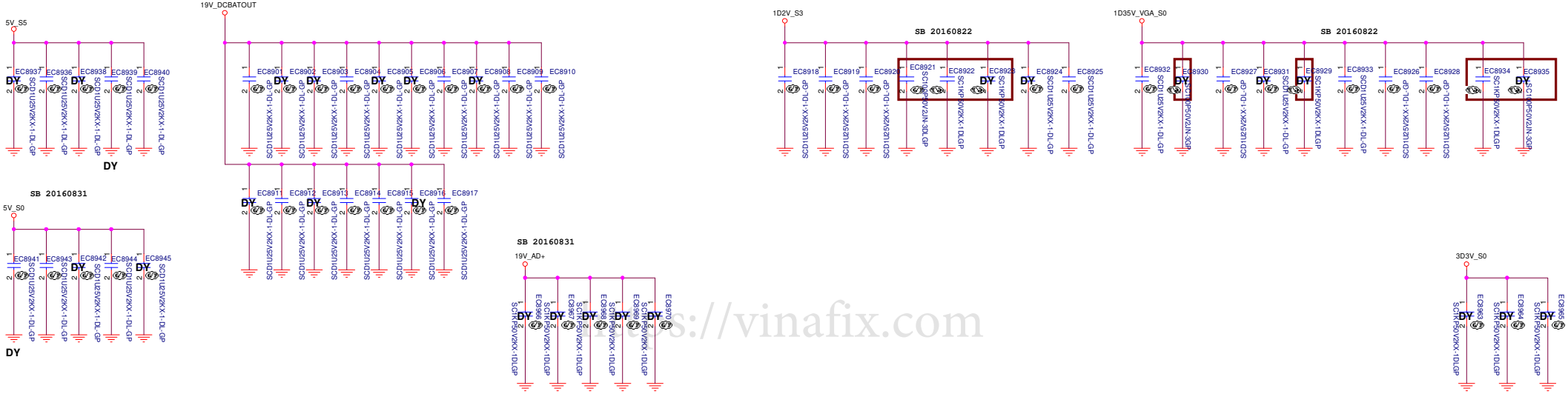
Main Func = UnusedParts



Main Func = EMI Capacitors



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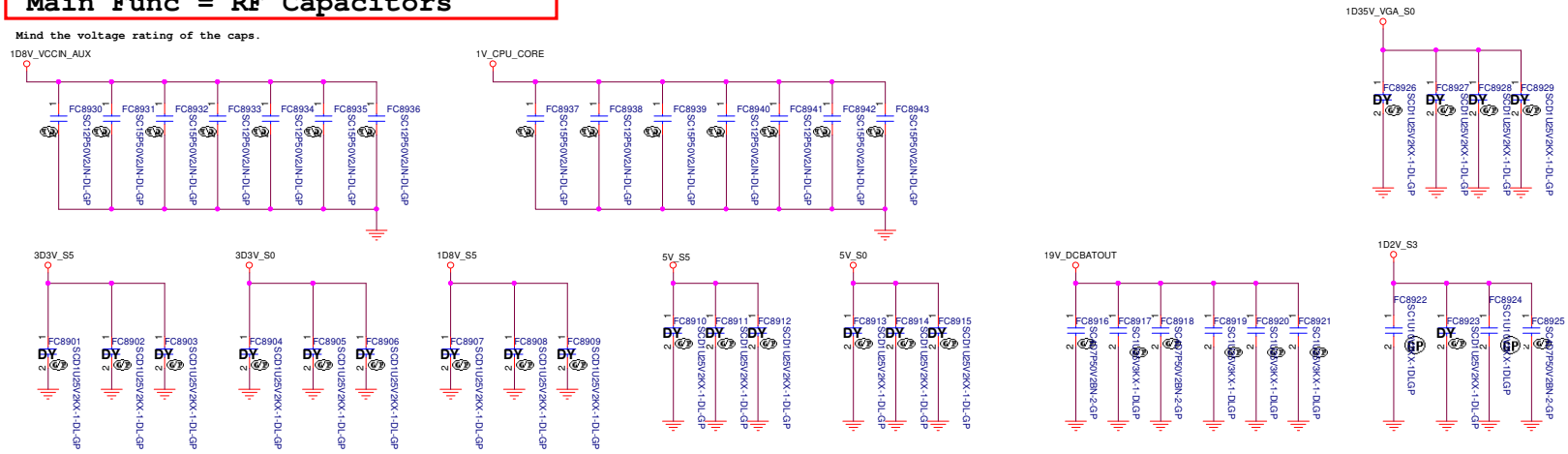
Main Func = RF Capacitors

Mind the voltage rating of the caps.



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Title: UNUSED PARTS (RF/EMI Capacitors)		
Size: Custom	Document Number: Cyborg_TGL-H RTX	Rev: X01
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Title: *INT IO (NFC/Camera/Touch)*

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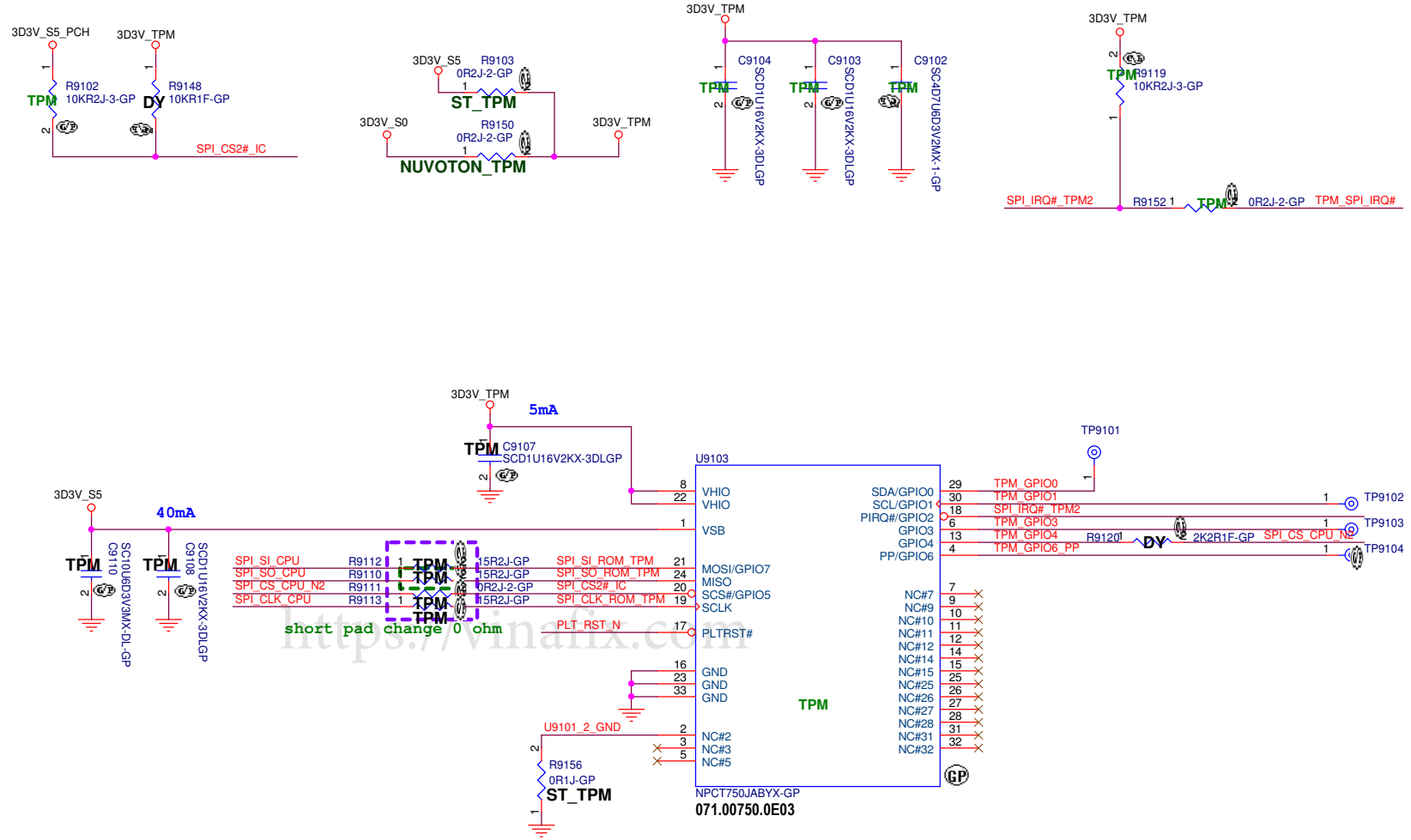
SSID = TPM

18,24,25 SPI_SO_CPU
18,24,25 SPI_CLK_CPU
11,18,24,25 SPI_SI_CPU
18 SPI_CS_CPU_N2

20,26,61,63,71,79 PLT_RST_N
20 PM_SLP_S0#

20 TPM_SPI_IRQ#

R9110.R9112.R9113	
SPI ROM	33 ohm 64.33R05.6DL
SHARE ROM	15 ohm 63.15034.1DL



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Title: INT IO (TPM)

Size: Custom | Document Number: Cyborg_TGL-H RTX | Rev: X01

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Title: INT IO (RSVD)

Size: A3 | Document Number: Cyborg_TGL-H RTX | Rev: X01

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Title *(RSVD)*

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Title	***(RSVD)***	
Size A3	Document Number **Cyborg_TGL-H RTX**	Rev **X01**
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title *(RSVD)*

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8/29 add XDP
9/26 3.3V(PU4501),DDR(PU5101),1.05V(PU5201)change to solution.

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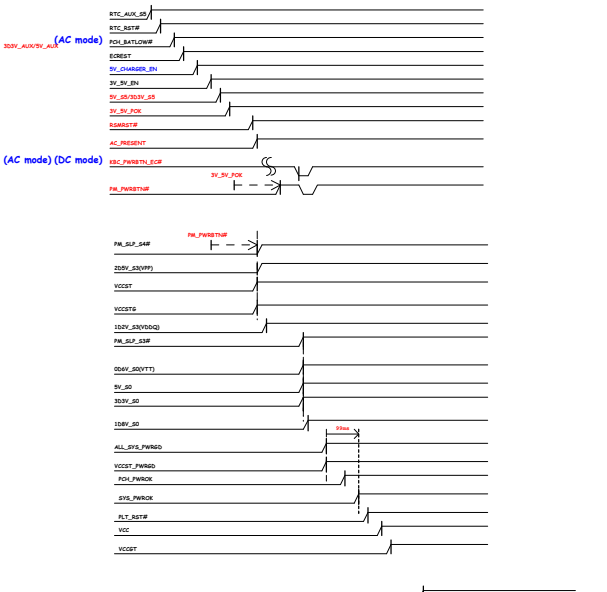
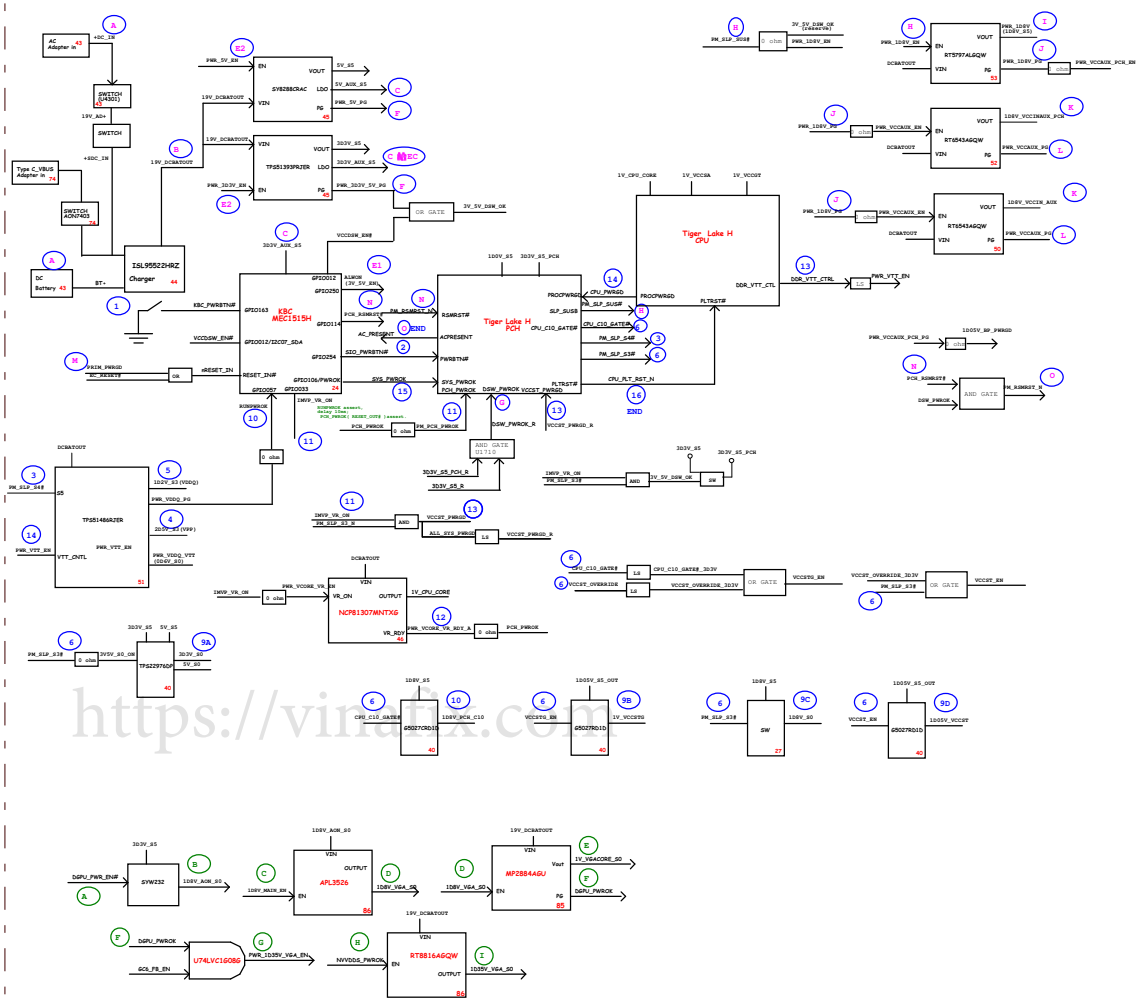
Intel-Power Up Sequence




AC Adapter in 43
SWITCH APL5931
SWITCH
Type C_VBUS Adapter in 74
SWITCH ADP4093
DC Battery 43
ISL9552HRZ Charger 44
SY8288CRAC
TPS51393RJER
OR GATE
KBC MEC1515H
Tiger Lake H FCH
Tiger Lake H CPU
RT5797ALGQW
RT6543AGQW
RT6543AGQW
TPS51486R2ER
MCP81307MNTXG
TPS22976DR
SYW232
APL3526
MP2884AGU
U74LVC1GO86
RT8816AGQW
AND GATE
SW
LS
LD
0 ohm
2K ohm
100K ohm
PWR_1D8V_EN
PWR_VCCAUX_EN
PWR_VTT_EN
PWR_VCCAUX_PCH_EN
PM_SLP_S3#
PM_SLP_S4#
PM_SLP_SUS#
PM_RSMRST#
PCH_RSMRST#
DSW_PWROK
SYS_PWROK
PCH_PWROK
PLT_RST#
CPU_PWRGD
CPU_C10_GATE#
VCCST_PWRGD
VCCST_OVERRIDE
VCCSTG_EN
VCCST_EN
1D8V_VCCIOMAUX_PCH
1D8V_VCCIOMAUX_AUX
1D8V_VCCSTG
1D8V_VCCST
1V_VGACORE_S0
1D8V_VGA_S0
1V_VCCSTG
1V_CPU_CORE
1V_VCCSA
1V_VCCST
DDR_VTT_CTL
DDR_VTT_EN
1D8V_XP_PWRGD
PCH_PWROK
DSW_PWROK
ALL_SYS_PWRGD
IMVP_VR_ON
PWR_VCORE_VR_EN
PWR_VCORE_VR_RDY_A
PWR_VDDQ_PG
PWR_VTT_EN
PWR_VDDQ_VTT
1D2V_S3(VDDQ)
2D5V_S3(VPP)
1D8V_S0
1D8V_S5
1D8V_S5_PCH
1D8V_S5_OUT
1D8V_AON_S0
1D8V_MAIN_EN
1D8V_VGA_S5
1D8V_PCH_C10
1D8V_VGA_S0
PWR_1D35V_VGA_EN
NVVDDS_PWROK
1D35V_VGA_S0
3D3V_S5
3D3V_AUX_S5
3D3V_S5_PCH
5V_S5
5V_AUX_S5
3V_5V_DSW_OK
VCCDSW_EN
PWR_5V_EN
PWR_3D3V_EN
PWR_5V_PG
PWR_3D3V_5V_PG
19V_DCBATOUT
19V_ADP
+3DC_IN
ACPRESENT
PWRBTN#
RSMRST#
SLP_SUS#
CPU_C10_GATE#
FLTRST#
PROCPWRGD
SYS_PWROK
RESET_IN#
KBC_PWRBTN#
VCCDSW_EN#
AC_PRESENT
SIO_PWRBTN#
PCH_RSMRST#
DSW_PWROK_R
VCCST_PWRGD_R
3D3V_S5_PCH_R
3D3V_S5_R
1D8V_S5_R
PCH_PWROK
PM_PCH_PWROK
PM_RSMRST_R
PM_SLP_SUS#
PM_SLP_S4#
PM_SLP_S3#
PM_SLP_S0#
PM_SLP_S0ix#
PM_SLP_SUS#
PM_SLP_S4#
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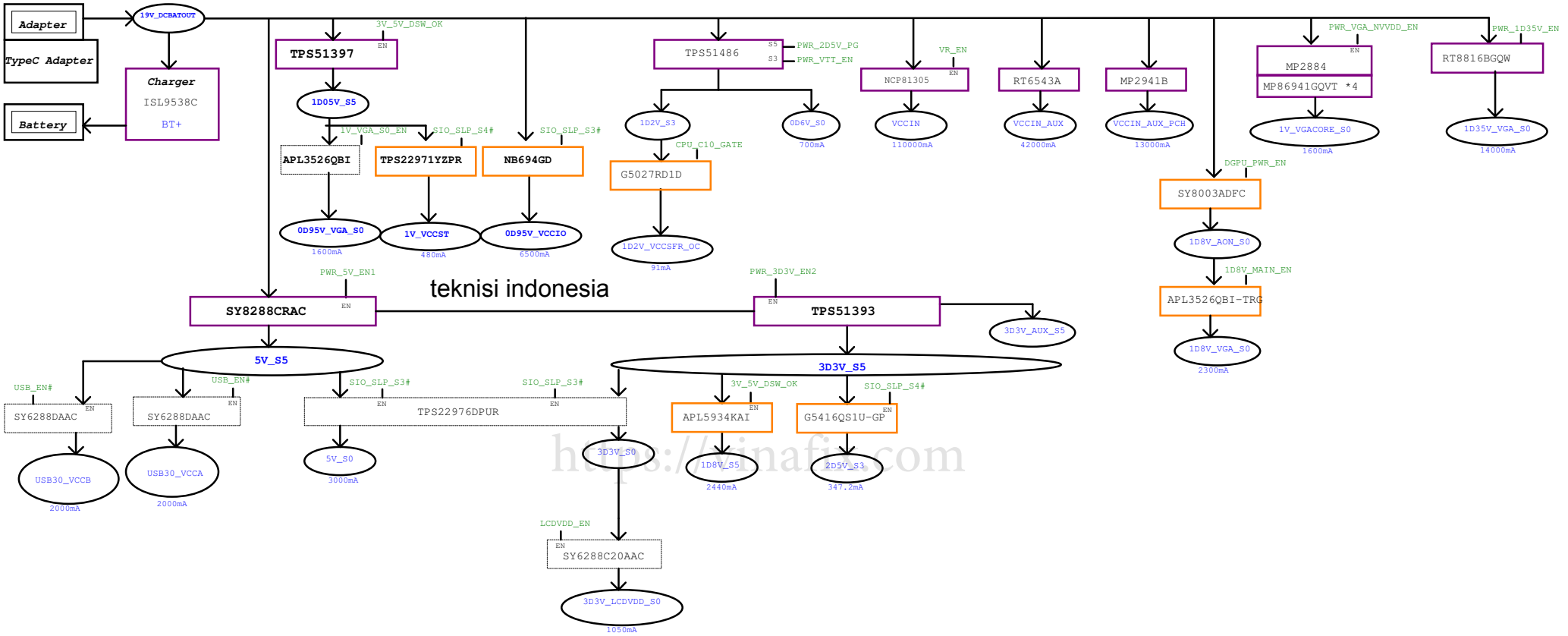
PM_SLP_S0ix#
PM_PWRBTN#
PM_RSMRST#
PM_PCH_PWROK



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Power Shape

Regulator | LDO | Switch

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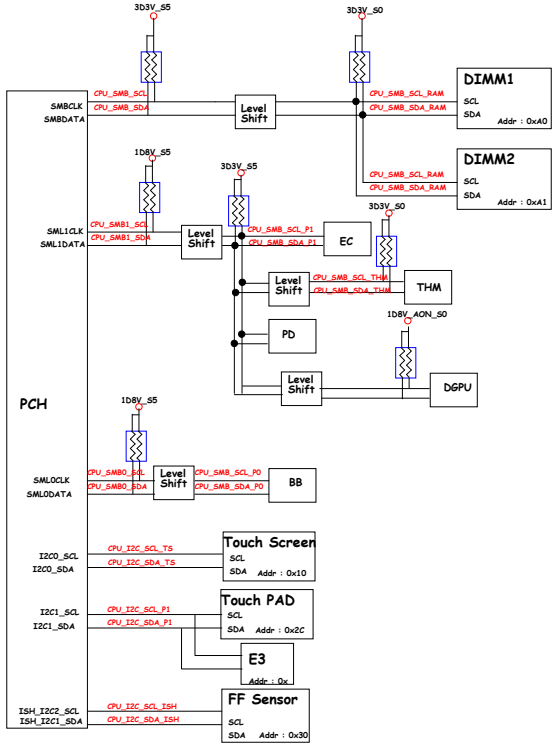
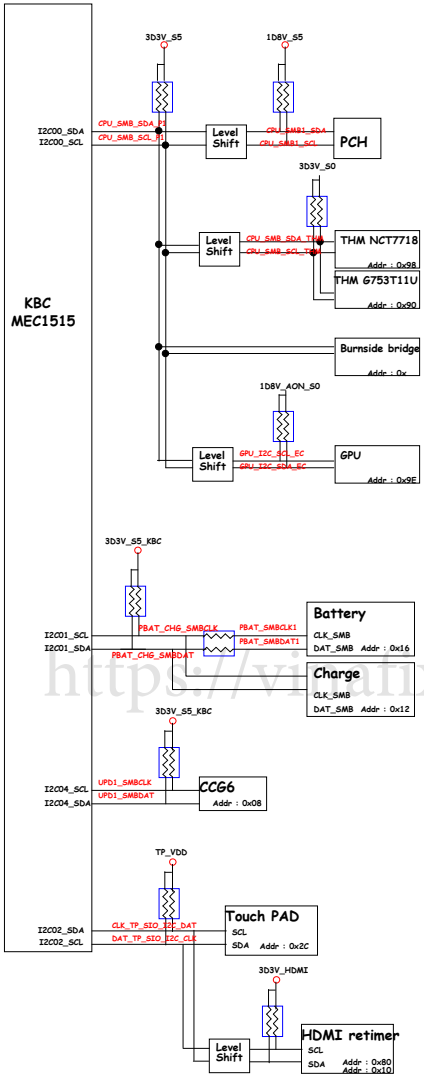
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS/I2C BLOCK DIAGRAM

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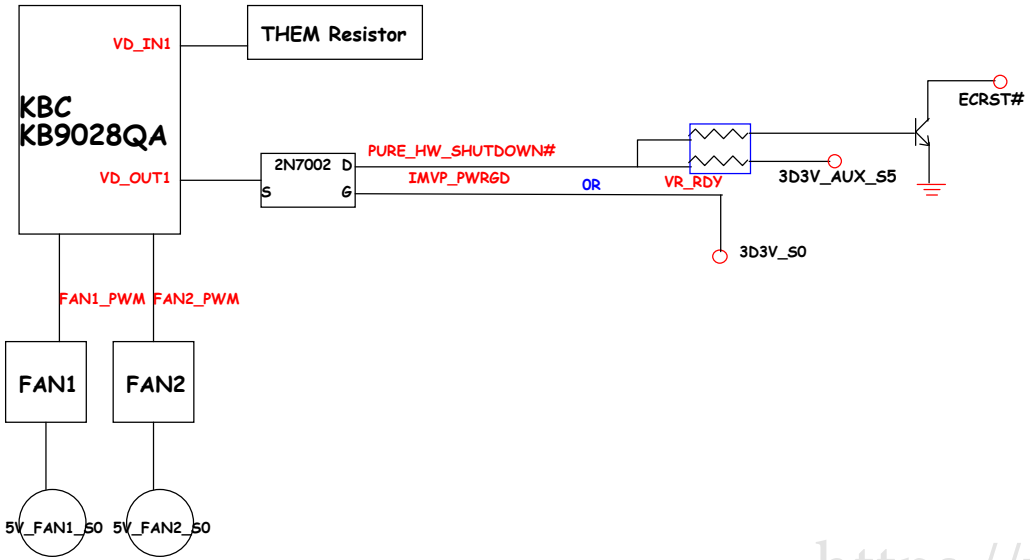
Thermal Block Diagram



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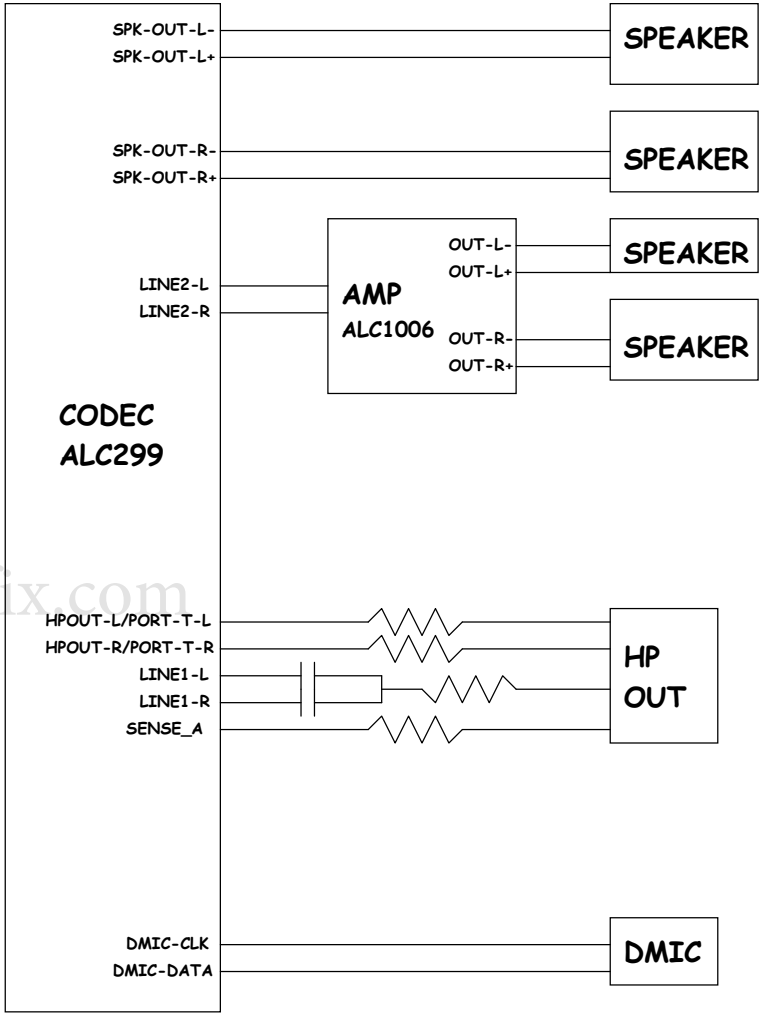
Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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